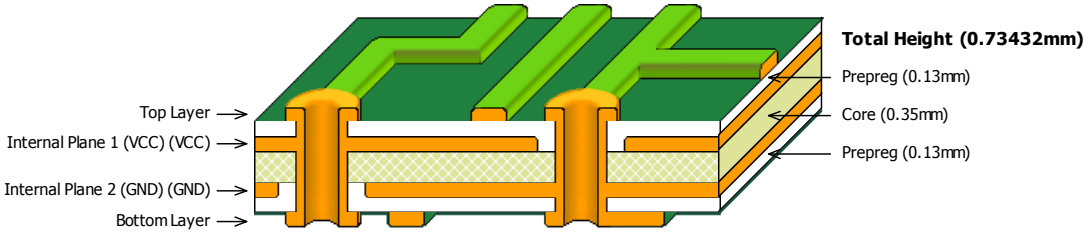
1 CuOF Tx1

1.1 PCB technology

The PCB layer stack is as follows:



Information is expanded in the corresponding pdf.

All signal tracks have a width of 8 mils, resulting in a ~50 Ω nominal impedance. Ground and bias tracks have a width of 50 mils.

1.2 Schematic and PCB conventions

All of the values for resistors and capacitors stated in the schematic have been chosen for some (possibly erroneous) reason. Non-specified values are either irrelevant, non-critical, or a priori unnecessary but placed to allow for modifications during the test phase.

Several *enable* inputs have been tied to a jumper+pull-up/down so that they can be easily modified. The regular (enabled) operation for all of them is with the jumper connected.

Several 2-pin connectors provide access to differential inputs and outputs. The connections have been made so that the pin with a square footprint corresponds to the positive conductor in the pair, and the pin with the circular footprint corresponds to the negative one. IMPORTANT: This only applies to the 2-pin connectors for diferential signals. It is not necessarily the case for others, and it is NOT for the power connector.

The jumpers can be distinguished from the signal 2-pin connectors in that the former retain the black plastic that keeps the two pins together while in the latter case it has been removed to ease the observation of the pad shape.

1.3 Bias circuit

The bias circuit is based on the MIC29151-3.3 voltage regulator, with capacitor-based voltage stabilization at both input and output. The power consumption is approximately 400 mA, depending on how many laser drivers are enabled.

Each IC has a nearby 100 nF bypass capacitor to stabilize and filter the bias.

Connectors for the power source are provided as well as pins for crimping to a cable. The polarity goes as follows: negative – top – square / positive – bottom – round.

1.4 Input connectors and channel selection

Signal input to the CuOF Tx1 can be done through one of the RJ-45 or the 2-pin connectors. The RJ-45 shield is ground-lifted through a 100 Ω, 1 W-rated resistor and a X7R

1.5 nF ceramic capacitor. The distribution of conductor pairs should be the cat-5E cable standard one.

The signals are routed to a 0603 footprint array in which one of the pairs can be selected by soldering a short circuit or an AC-coupling capacitor (~100 nF). Each pair is length-matched (different pairs are not matched between each other) to better preserve eye integrity.

1.5 Equalizer impedance termination/matching

Input differential pairs have been terminated according to the equalizer and LVDS specifications. However, several footprints have been added to ease modifications to fine-tune the adaptation.

- LMH0024: input is self-biased, high impedance, so the input stage should, theoretically, consist in a pair of AC-coupling capacitors and a 100 Ω differential termination. A serial (short-circuited) footprint and two parallel pull-up/down resistors have also been included.

- MAX3800: input is self-biased, with single-ended 50 Ω termination. Thus, input should consist in a pair of AC-coupling capacitors. Two parallel (pull-up/down) and series (short-cirucited) footprints have also been included. In fact, the pull-down footprints have been used to add 33 pF capacitors that improve signal integrity.

Regarding output impedance matching, it's worth mentioning that the nominal output impedance of the MAX3800 equalizer is 62.5 Ω, single-ended, which may produce reflections when connected to the 50 Ω tracks. In case this poses a problem, two series 0603 short-circuited footprints have been included so that 12 Ω resistors can be soldered. Right now, these two footprints are being used to cross the two channels, because due to an error in the schematic design, the output p and n pads are inverted.

1.6 Inter-connection matrix

The interconnection matrix has been designed as a bi-dimensional array of 0603 footprints, so that any of the three input stages can bee connected to any of the three laser drivers. The connection can be made by soldering AC-coupling capacitors in the appropriate positions.

The rows correspond to each of the laser drivers:

First row (P10)	MAX3643 (U5)
Second row (P12)	MAX3646 (U6)
Third row (P14)	SY88216 (U7)

The columns correspond to each of the three equalizers. Each column is marked with a number to its right that is the number of its corresponding equalizer's component designator (Ux):

Columns 1 and 6 (marked "4" and "")	MAX3800 (U4)
Columns 2 and 5 (marked "3")	LMH0024-bottom (U3)
Columns 3 and 4 (marked "1")	LMH0024-top (U1)

Each differential pair of tracks leaving or arriving to the inter connection matrix is length-matched.

1.7 Laser drivers/diodes

The three output stages make use of one HFE4190 laser driver from finisar, whose typical resistance under normal operation conditions is 35 Ω. The laser drivers are designed to work with 5 Ω laser diodes, and since our VCSEL is 35 Ω we have compensated the extra impedance reducing the series resistors in the OUT+ and BIAS+ outputs. For the moment we haven´t spotted major problems due to that. All of the laser drivers have some status monitoring outputs (either open-circuit or with a resistive load) that can be accessed.

1.7.1 MAX3643

- Input matching: high impedance, non biased → 82 Ω/130 Ω pull-up/down for proper termination and biasing.
- BEN inputs: this laser driver allows burst-mode operation, controlled by LVPECL inputs. These inputs are pulled up/down with 1k resistors so that Burst is always on, although the footprints for two voltage dividers are included in case this solution does not work correctly.
- EN* tied low by the jumper.
- Configured so that Ibias = 5.3 mA, Imod = 7 mA, Imax = 18 mA

1.7.2 MAX3646

- Input matching: high impedance, biased → 100 Ω differential termination.
- TX_DISABLE tied low by the jumper.
- Capc = 1 uF → cutoff frequency ~700 kHz. This is ~400 times slower than the 240 Mbps transmission rate, in order to minimize interaction with low frequency in the data pattern.
- Configured so that Pavg = 0.5 mW, no temperature compensation, Imod = 12 mA (Ibias is determined through the Monitor diode feedback).

1.7.3 SY88216

- Input matching: 50 Ω termination, biased → direct connection (through AC-coupling capacitors).
- EN* tied low by the jumper.
- BEN inputs: same as with MAX3643.
- Configured so that Imd = 0.5 mA (Pavg = 0.5 mW), Ibias < 5 mA, Imod = 7 mA. The two latter conditions are imposed by resistor values extrapolated from the datasheet typical operation conditions graphs → I guess they're not guaranteed to work as I expect them to.

After calculating the working values, some tweaking and optimization in resistor values was carried out, and for this reason the values stated in the schematic may seem not to be the

appropriate to configure the device as described in this document. The schematic reflects (hopefully without errors) the actual values of the boards as we sent them.

2 CuOF Rx1

In order to evaluate the different transmitter configurations, a CuOF Rx1 board is also sent. Most of the general information about CuOF Tx1 also applies here (PCB technology, conventions, bias …).

2.1 LVDS Buffer

A 4-Channel 800 Mbps LVDS Buffer/Repeater has been included in order to be able to make differential signal conversion. Two of the channels are AC-coupled at their inputs with 10 nF capacitors.

2.2 Finisar transceiver

A Finisar FTLF8519F2GCL transceiver has been included, in order to be able to receive the optical signal. The biasing stabilization network includes two electrolytic parallel capacitors, and two 60 Ω ferrite beads followed by their corresponding capacitors.

The transmitter's disable can be tied low with a jumper.

2.3 RJ45 connector

A RJ45 connector with fan-out to its four differential channels is provided, in case it is necessary to introduce the received differential signal into any of its pairs. It is ground-lifted in the same way as in the CuOF Tx1 board.

3 Results

Little characterization has been done yet on the complete system. We have initially evaluated the LMH0024 + MAX3643 combination, with the finisar receiver.

An initial BER test, running for approximately 4 hours, revealed a BER of approximately 7·10–11. However, errors appear to occur in bursts, so it is probable that these had something to do with external perturbations in the lab. This suggests that the steady-state BER would be a lot better, but also that the system as it is right now may not be very robust to bias instability/ EMI, of which we will have plenty in operation at CMS.

Further characterization shows that there is a 50 minute period in these error bursts. Also, we have verified that the bias network in our FPGA evaluation board makes the data reception considerably sensitive to perturbations in the power lines. Our conclusion is that the BER of the system is significantly lower than the one we have measured, but that we are unable to better delimit it with our current system, due to the instability of the power lines.

The total delay caused by the Cu-OF and OF-Cu conversion is approximately 3.5 ns, which seems acceptable in terms of trigger latency restrictions.