Ciemat Centro de Investigaciones Energéticas, Medioambientales y Tecnológicas

VME_PATCH
User Manual

Version 3.0

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1 VME_PATCH BOARD

The goal of this board is to perform the bridge between the VME controller of the ROS and TSC crates (usually Linco VME controller) and the OFCU and TSC_rear modules.

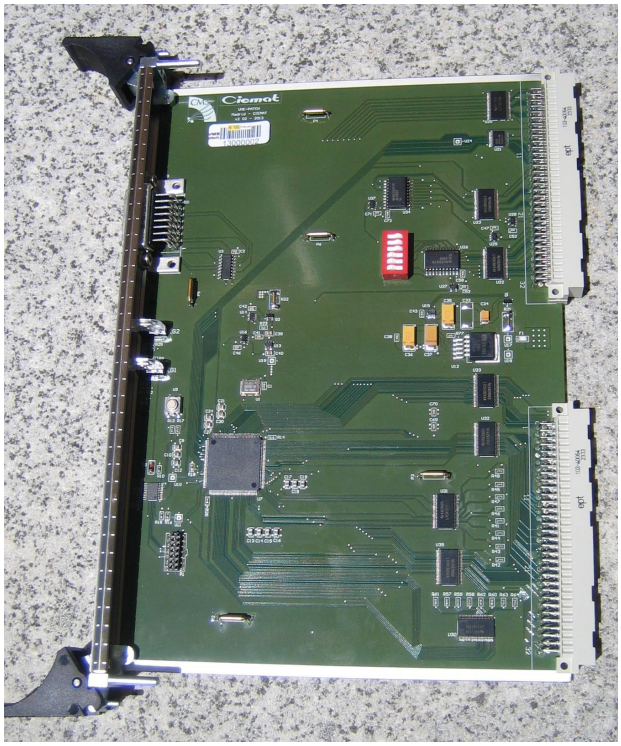

Figure 1: Front image of the VME_PATCH board.

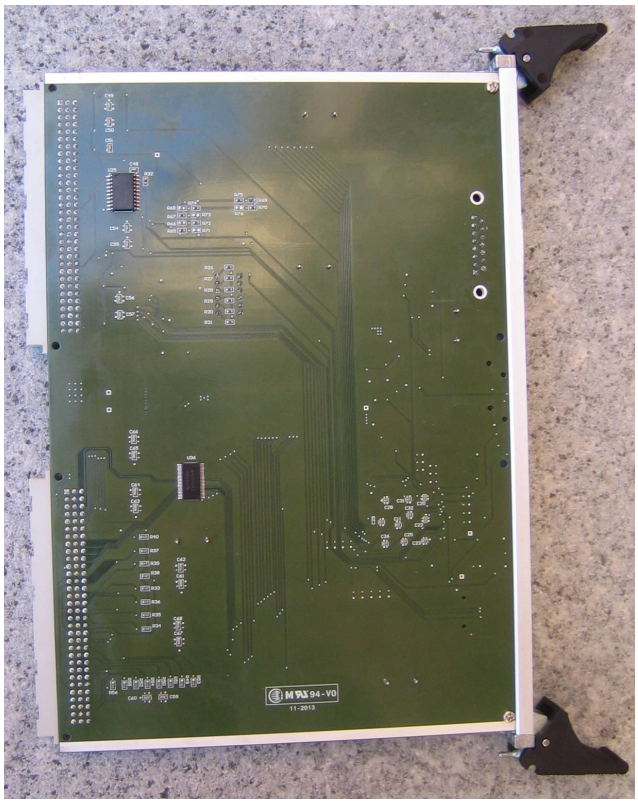

Figure 2: Back image of the VME_PATCH board.

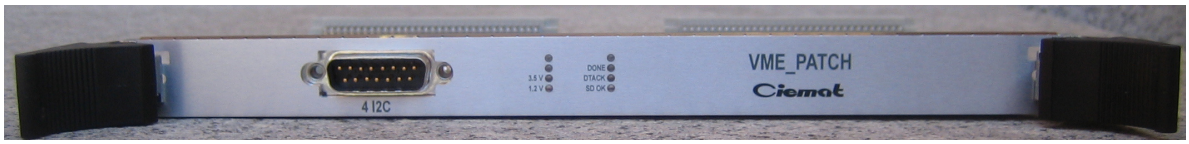

Figure 3: Image of the VME_PATCH front pannel

2 VME_PATCH INTERFACES

The front panel has:

- DA-15 male connector that contains four I^2C buses with the following mapping:

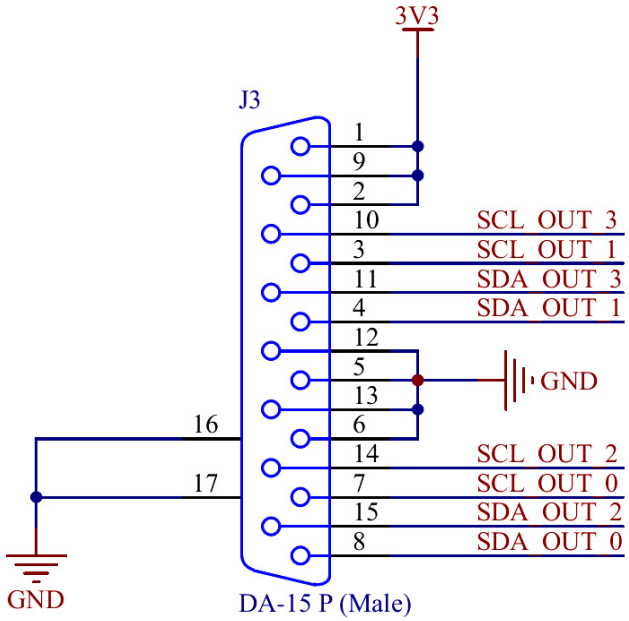

Figure 4: I^2C DA-15 P male connector

Note that the corresponding DA-15 female socket must have the pin-out mirrored:

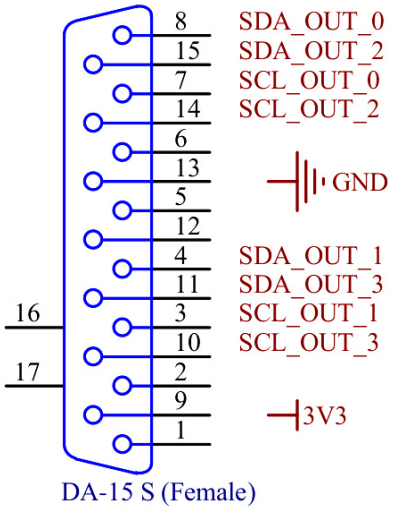

Figure 5: I^2C DA-15 S female socket

- First row of leds. From left to right:
  - ON = 1.2 V ok [D5 = 1.2 V]
  - ON = 3.3 V ok [D6 = 3.5 V]

- Second row of leds. From left to right:
  - ON = All signal detects of the OFCU boards in the crate are OK [D1 = SD OK]
  - ON = VME access data acknowledge of the VME_patch [D3 = DTACK]
  - ON = VME_patch FPGA properly programmed (done) [D4 = DONE]

The backplane connections contain a J1 VME standard connector and a custom J2 to connect to the J2_OFCU backplane. The J2 mapping is (the signals in grey do not exist at present):

VME PATCH	A	B	C
1	Sp_indiv_1	V_5	SD_1_1
2	Sp_indiv_2	GND	SD_1_2
3	Sp_indiv_3	SD_10_1	SD_1_3
4	Sp_indiv_4	SD_10_2	SD_2_1
5	Sp_indiv_5	SD_10_3	SD_2_2
6	GND	SD_11_1	SD_2_3
7	Sp_indiv_6	SD_11_2	SD_3_1
8	Sp_indiv_7	SD_11_3	SD_3_2
9	Sp_indiv_8	SD_12_1	SD_3_3
10	Sp_indiv_9	SD_12_2	SD_4_1
11	Sp_indiv_10	SD_12_3	SD_4_2
12	Board_sel1	GND	SD_4_3
13	Board_sel2	V_5	SD_5_1
14	Board_sel3	Reset	SD_5_2
15	Board_sel4	ADD_0	SD_5_3
16	Board_sel5	ADD_1	SD_6_1
17	Board_sel6	ADD_2	SD_6_2
18	V_5	ADD_3	V_5
19	GND	Spare_5	GND
20	Board_sel7	Write_J2	SD_6_3
21	Board_sel8	Sp_indiv_11	SD_7_1
22	Board_sel9	GND	SD_7_2
23	Board_sel10	Dout_0	SD_7_3
24	Board_sel11	Dout_1	SD_8_1
25	Board_sel12	Dout_2	SD_8_2
26	V_5	Dout_3	V_5
27	GND	Dout_4	GND
28	Spare_0	Dout_5	SD_8_3
29	Spare_1	Dout_6	SD_9_1
30	Spare_2	Dout_7	SD_9_2
31	Spare_3	GND	SD_9_3
32	Spare_4	V_5	Sp_indiv_12

Figure 6: J2 VME_patch mapping

The schematics of the VME_PATCH board can be found here:

http://wwwae.ciemat.es/cms/DTE/iupgrade.htm#VMEpatch

3 VME_PATCH ADDRESSING

The VME_PATCH board supports short non-privileged A16 D16 (Word) VME access. It translates it to the OFCU boards by means of a custom parallel protocol.

The A16 base address is selected with switch SW13, (A15-A10).
The address mapping for the registers of the different functional blocks is what follows:

A16 Base Address (A15 – A10)	Functional block
VME_PATCH + 0x00 a 0x3E	VME_PATCH
VME_PATCH + 0x40 a 0x5E	OFCU slot 1
VME_PATCH + 0x80 a 0x9E	OFCU slot 2
VME_PATCH + 0xC0 a 0xDE	OFCU slot 3
VME_PATCH + 0x100 a 0x11E	OFCU slot 4
VME_PATCH + 0x140 a 0x15E	OFCU slot 5
VME_PATCH + 0x180 a 0x19E	OFCU slot 6
VME_PATCH + 0x1C0 a 0x1DE	OFCU slot 7
VME_PATCH + 0x200 a 0x21E	OFCU slot 8
VME_PATCH + 0x240 a 0x25E	OFCU slot 9
VME_PATCH + 0x280 a 0x29E	OFCU slot 10
VME_PATCH + 0x2C0 a 0x2DE	OFCU slot 11
VME_PATCH + 0x300 a 0x31E	OFCU slot 12

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						J2_3	J2_2	J2_1	J2_0						Vme BYTE

4 VME_PATCH BOARD REGISTERS

Reg1_vme (VME_PATCH + 0x00)

Default value = 0x0
Reset by a local_reset.

Bits	**description**	**acc**	
0-2	Dummy	R/W	
3	Lights SD LED	R/W	Turns on the SD led in the front panel of the VME_patch even if the SD signals are not correct
4	Read _J2	R/W	Sets the line Read_J2
5	Spare _J2	R/W	Sets the line Spare _J2
6	OFCU Reset	W	=1 reset (100 ns pulse). A reset will be sent sequentially to each OFCU.
7	Local_reset	W	=1 reset of the VME_PATCH board only

All the registers from VME_PATCH are reset by a local reset.
A VME sys-reset will force also a reset in the VME_PATCH and in the OFCU boards.

Interruptions_Set (VME_PATCH + 0x02)

Default value = 0x0
Reset by a local_reset.

Bits	**description**	**acc**	
0	enable test interrupt	R/W	= 1 an interruption will be generated
1	interrupt requested	R	= 1 an interruption from the VME_PATCH has occurred.
2-7	Dummy	R/W	

Interruptions_Vector (VME_PATCH + 0x04)

Default = 0x0
Reset by a local_reset.

Bits	**Description**	**acc**	
0-7	interrupt vector	R/W	

Interrupt Level is always 7

SCL (VME_PATCH + 0x06)

Default = 0x1
Reset by a local_reset.

Bits	**Description**	**acc**	
0	SCL write	W	SCL signal. The I2C bus you are addressing is selected in register I2C select.
1	SCL read	R	SCL signal registered each clock cycle. The I2C bus you are addressing is selected in register I2C select (0x0A)
2-7	'0'	-	

SDA (VME_PATCH + 0x08)

Default = 0x1
Reset by a local_reset.

Bits	**Description**	**acc**	
0	SDA write	W	SDA signal. The I2C bus you are addressing is selected in register I2C select (0x0A)
1	SDA read	R	SDA signal registered each clock cycle. The I2C bus you are addressing is selected in register I2C select (0x0A)
2-7	'0'	-	

I²C SELECT (VME_PATCH + 0x0A)

Default = 0x0
Reset by a local_reset.

Bits	Description	acc	
0	A0 – selection of I^2C bus to address	R/W	
1-3	-	-	
4	A1 – selection of I^2C bus to address	R/W	
5-7		-	

0x00 => SDA0, SCL0
0x01 => SDA1, SCL1
0x10 => SDA2, SCL2
0x11 => SDA3, SCL3

SIGNAL DETECT OFCU 1-2 (VME_PATCH + 0x0C)

Default = 0x0
Reset by a local_reset.

bits	Description	acc
0	Signal Detect OFCU=1, ROS ch 0-11 MB1and MB2	R
1	Signal Detect OFCU=1, ROS ch 12-23 MB3and MB4	R
2	Signal Detect OFCU=1, ROS ch 24 (single) MB4-b last	R
3	Signal Detect OFCU=2, ROS ch 0-11 MB1and MB2	R
4	Signal Detect OFCU=2, ROS ch 12-23 MB3and MB4	R
5	Signal Detect OFCU=2, ROS ch 24 (single) MB4-b last	R
6-7	-	

SIGNAL DETECT
= 1 MEANS ALL OK (OFCU board connected, Avagos in, signal received)
=0 MEANS THERE IS A CHANNEL THAT IS IN NOT RECIVING SIGNAL

SIGNAL DETECT OFCU 3-4 (VME_PATCH + 0x0E)

Default = 0x0
Reset by a local_reset.

bits	Description	acc
0	Signal Detect OFCU=3, ROS ch 0-11 MB1and MB2	R
1	Signal Detect OFCU=3, ROS ch 12-23 MB3and MB4	R
2	Signal Detect OFCU=3, ROS ch 24 (single) MB4-b last	R
3	Signal Detect OFCU=4, ROS ch 0-11 MB1and MB2	R
4	Signal Detect OFCU=4, ROS ch 12-23 MB3and MB4	R
5	Signal Detect OFCU=4, ROS ch 24 (single) MB4-b last	R
6-7	-	

SIGNAL DETECT OFCU 5-6 (VME_PATCH + 0x10)

Default = 0x0
Reset by a local_reset.

bits	Description	acc
0	Signal Detect OFCU=5, ROS ch 0-11 MB1and MB2	R
1	Signal Detect OFCU=5, ROS ch 12-23 MB3and MB4	R

2	Signal Detect OFCU=5, ROS ch 24 (single) MB4-b last	R
3	Signal Detect OFCU=6, ROS ch 0-11 MB1and MB2	R
4	Signal Detect OFCU=6, ROS ch 12-23 MB3and MB4	R
5	Signal Detect OFCU=6, ROS ch 24 (single) MB4-b last	R
6-7	-	

SIGNAL DETECT OFCU 7-8 (VME_PATCH + 0x12)

Default = 0x0
Reset by a local_reset.

bits	Description	acc
0	Signal Detect OFCU=7, ROS ch 0-11 MB1and MB2	R
1	Signal Detect OFCU=7, ROS ch 12-23 MB3and MB4	R
2	Signal Detect OFCU=7, ROS ch 24 (single) MB4-b last	R
3	Signal Detect OFCU=8, ROS ch 0-11 MB1and MB2	R
4	Signal Detect OFCU=8, ROS ch 12-23 MB3and MB4	R
5	Signal Detect OFCU=8, ROS ch 24 (single) MB4-b last	R
6-7	-	

SIGNAL DETECT OFCU 9-10 (VME_PATCH + 0x14)

Default = 0x0
Reset by a local_reset.

bits	Description	acc
0	Signal Detect OFCU=9, ROS ch 0-11 MB1and MB2	R
1	Signal Detect OFCU=9, ROS ch 12-23 MB3and MB4	R
2	Signal Detect OFCU=9, ROS ch 24 (single) MB4-b last	R
3	Signal Detect OFCU=10, ROS ch 0-11 MB1and MB2	R
4	Signal Detect OFCU=10, ROS ch 12-23 MB3and MB4	R
5	Signal Detect OFCU=10, ROS ch 24 (single) MB4-b last	R
6-7	-	

SIGNAL DETECT OFCU 11-12 (VME_PATCH + 0x16)

Default = 0x0
Reset by a local_reset.

bits	Description	acc
0	Signal Detect OFCU=11, ROS ch 0-11 MB1and MB2	R
1	Signal Detect OFCU=11, ROS ch 12-23 MB3and MB4	R
2	Signal Detect OFCU=11, ROS ch 24 (single) MB4-b last	R
3	Signal Detect OFCU=12, ROS ch 0-11 MB1and MB2	R
4	Signal Detect OFCU=12, ROS ch 12-23 MB3and MB4	R
5	Signal Detect OFCU=12, ROS ch 24 (single) MB4-b last	R
6-7	-	

OFCU_RESET (VME_PATCH + 0x18)

Default = 0x0
Reset by a local_reset.

bits	Description	acc
0-7	OFCU Slot to which a reset wants to be issued (75 ns reset pulse)	R/W

The number you write here is the OFCU slot (i.e. sector) to which a reset will be sent. 0x1 to reset OFCU from sector 1, 0x5 to reset OFCU sector 5, etc.

5 ACCESSING THE CUOF MEZZANINE

The VME_PATCH board can be used to access the CUOF mezzanine for configuration through the DA-15 connector in the front of the board.

You need to connect a cable like the one in the picture to each of the individual pseudo-I^2C channels. Alternatively, you can make an OR of all the lines from the 8 laser drivers in the CUOF mezzanine and access all of them simultaneously (clearly, the same bias/modulation parameters will be configured for all of the laser drivers).

Writing in the I^2C_SELECT register of the VME_PATCH you can choose which of the 4^{th} channels is going to be used for the I^2C transmission. In addition writing in the SDA and SCL registers, you can send the appropriate commands. An example of the software to be used can be found here:

http://wwwae.ciemat.es/cms/DTE/iupgrade.htm#VMEpatch