ROB-testing setup documentation

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Patgen

Overview

The patgen board makes a fan-out of two different input pulse signals to the 128 channels that a ROB can measure. The patgen board is controlled through 17 registers that can be read and written through the VME bus interface.

The patgen board has 5 different XILINX XC95144XL CPLD's. Four of them are used for the fan out of the pulse signals (patgen CPLD from now on), which is a task that consumes a high number of terminals in each one of them. The fifth is devoted to VMEbus control tasks (pgvme CPLD from now on).

Each one of the CPLD's can be re-programmed through the JTAG interface, for which the TMS, IDT, TDO, TCK, GND and VCC are available.

In each of the CPLD's, four test points have been made easily electrically accessible, for simple signal monitoring during the debugging process. These correspond to ph(0-3) outputs in the VHDL description.

The clock for the CPLD's is generated by a a 40 MHz cristal oscillator which is distributed to the five CPLD's through a CY2309ZC-1H zero-delay buffer.

The output signals are converted from the LVTTL generated by the corresponding CPLD to a LVDS by 32 DS90C031 quad CMOS differential line drivers. These signals are outputted through four 68-pin connectors, each carrying the signal corresponding to 32 channels to the ROB.

The address the patgen board responds to is set by an array of DIP switches, that set the 10 most significant bits of the VME address in A16 addressing mode (A15-A6).

All of the relevant VMEbus signals are connected to the pgvme CPLD, except for the lower 16 bits of the data bus, which are connected to all four of the patgen CPLD's through a 74LVT16245 low voltage 16-bit transceiver with 3-state outputs, to allow for bidirectional communication. The patgen board control registers are, thus, stored in the corresponding patgen CPLD, and are written to/read from without passing through the pgvme CPLD.

The patgen board accepts two different LVDS inputs. These signals are converted into LVTTL by a a DS90LV048 line receiver, and passed to the four patgen CPLD's.

The power is regulated by a MIC29151 3.3V voltage regulator, which is protected by a a MAX869L current-limited, high-side p-channel switch with thermal shutdown.

Control Registers

The patgen board has 17 registers to control the way the fan-out of the two input pulses is done.

Each channel has two associated control bits, corresponding to the pulse 0 and pulse 1 inputs, that can be set independently in different registers. The output of channel i can be written as:

```
(channel i output) =    ( (pulse0) AND (channel i pulse0 control bit) ) OR
                        ( (pulse1) AND (channel i pulse1 control bit) )
```

Or, in words, at any time a active level in any of the pulse input generates an active level in the output if the corresponding control bit is set.

The registers are:

`Register  0 (0x00) 0 0 0 0 0 / ce0`

0-15	Pulse 0 - bits 0-15	R/W

`Register  1 (0x02) 0 0 0 0 1 / ce0`

0-15	Pulse 0 - bits 16-31	R/W

`Register  2 (0x04) 0 0 0 1 0 / ce1`

0-15	Pulse 0 - bits 32-47	R/W

`Register  3 (0x06) 0 0 0 1 1 / ce1`

0-15	Pulse 0 - bits 48-63	R/W

`Register  4 (0x08) 0 0 1 0 0 / ce2`

0-15	Pulse 0 - bits 64-79	R/W

`Register  5 (0x0A) 0 0 1 0 1 / ce2`

0-15	Pulse 0 - bits 80-95	R/W

`Register  6 (0x0C) 0 0 1 1 0 / ce3`

0-15	Pulse 0 - bits 96-111	R/W

`Register  7 (0x0E) 0 0 1 1 1 / ce3`

0-15	Pulse 0 - bits 112-127	R/W

`Register  8 (0x10) 0 1 0 0 0 / ce0`

0-15	Pulse 1 - bits 0-15	R/W

`Register  9 (0x12) 0 1 0 0 1 / ce0`

0-15	Pulse 1 - bits 16-31	R/W

`Register 10 (0x14) 0 1 0 1 0 / ce1`

0-15	Pulse 1 - bits 32-47	R/W

`Register 11 (0x16) 0 1 0 1 1 / ce1`

0-15	Pulse 1 - bits 48-63	R/W

`Register 12 (0x18) 0 1 1 0 0 / ce2`

0-15	Pulse 1 - bits 64-79	R/W

`Register 13 (0x1A) 0 1 1 0 1 / ce2`

0-15	Pulse 1 - bits 80-95	R/W

`Register 14 (0x1C) 0 1 1 1 0 / ce3`

0-15	Pulse 1 - bits 96-111	R/W

`Register 15 (0x1E) 0 1 1 1 1 / ce3`

0-15	Pulse 1 - bits 112-127	R/W

`Register 16 (0x20) 1 0 0 0 0`

1	Reset	W

For each register, the address shift is given in parenthesis (it is double the register number since they are accessed at word level). After each register, a ceX code is given: it refers to which of the four patgen CPLD's in the patgen board is in charge of the management and operation of this register.

(+) FALTA DECIR A QUÉ BIT DE LA ROB SE REFIERE CADA BIT DE LOS REGISTROS.

VMEbus interface

The VMEbus interface in the patgen board is controlled by the pgvme CPLD, and the registers are stored in the patgen CPLD's. The interface has been designed to work under the following specifications:

- Addressing: as the A16 mode is used, address bits A01 – A15 will be used.
  - Address modifier code (AM5 … AM0) = 101x01, or hex codes 0x29 or 0x2D, which corresponds to short access (A16) either supervisory or non-privileged mode (no distinction is made).
  - IACK* = 1
- Data mode: aligned D16 access is used.
  - LWORD* = 1
  - DS0* = DS1* = 0 while bus data bits are being operated.

In order for the patgen board to work correctly in systems where address pipelining is in use, the address bits are latched when DS0* falls to 0, and the information in AS* it is not used at all (Note: it probably should be latched when any data strobe falls, possible VHDL error?).