Centro de Investigaciones Energéticas, Medioambientales y Tecnológicas

ROS-25 User Manual

Version 4.1

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Electrónica y Automática.
CIEMAT.

Changes firmware 2010 in red
Changes firmware 2011 in green
Changes firmware 2012 in blue
Changes firmware MAY 2012 in violet
Changes firmware MARCH 2015 in orange

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1 INTRODUCTION

In this manual it is explained the basic functionality of the Read-Out Server (ROS) board. This board performs the second level of read-out in the data acquisition chain of the muon drift tube system of CMS. Its main task is the management of digitalized data that comes from the Read-Out Boards (ROB), located inside the Minicrates, attached to the drift tube chambers. Each ROS board can handle up to 25 input channels (up to 25 ROBs), storing data and performing a data merging event by event for further optical transmission to next level of the DAQ chain, the DDU.

In the following figure, a general scheme of the read-out chain of the drift tubes sub-detector is presented:

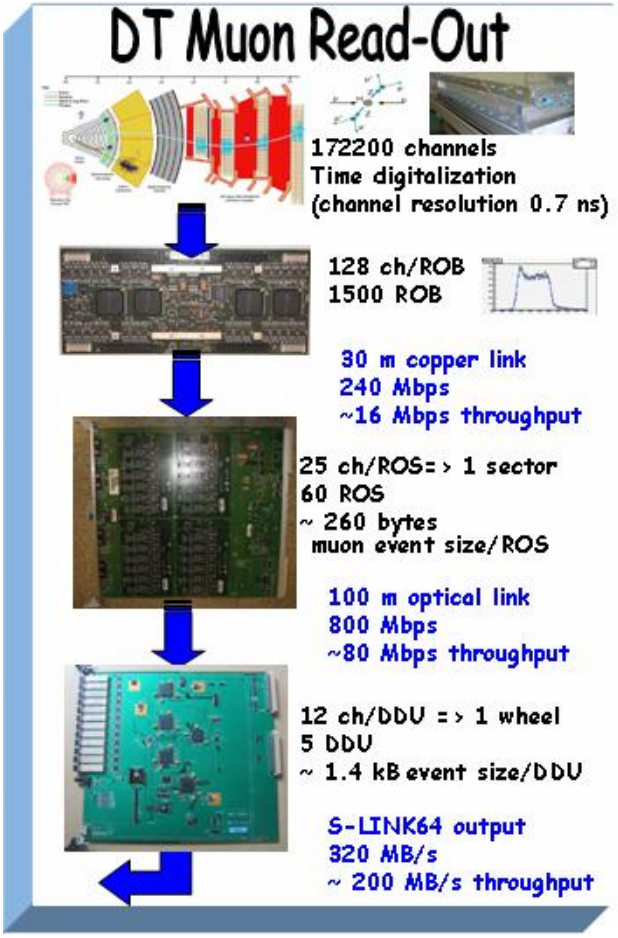

Figure 1: Diagram of the Drift Tubes read-out chain.

The ROS board is a 9U VME board, 400 mm depth with 8 RJ-45 input connectors and one optical output. Apart from transmission of received data through the optical output, the ROS has a spy memory where a programmed amount of events can be stored for further reading through a VME interface.

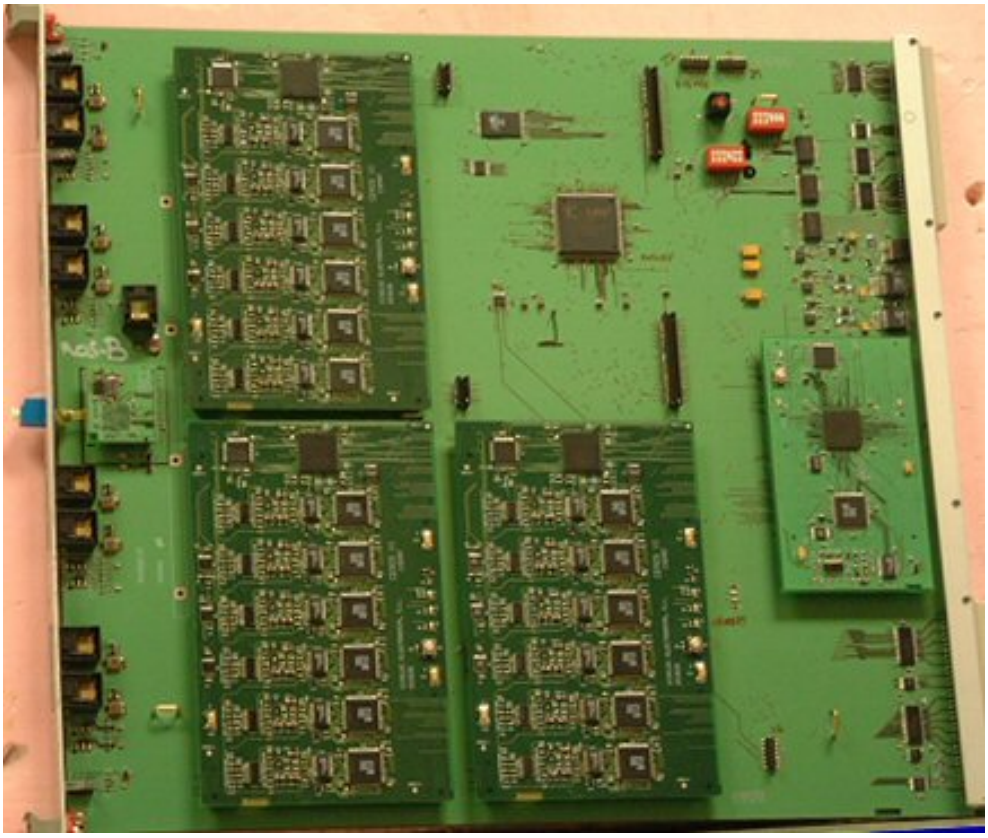

Figure 1: Picture of a Read-Out Server board.

2 ROS-25 CONNECTIONS

ROS boards will be located in two crates (TOP and BOTTOM) of the DT & RPC TRIGGER RACK (X2J22, X2J12, X2J02, X2V12, X2V22), that is, the outer rack of the lowest near balcony of each wheel. There will be 6 ROS per crate, named from ROS1 to ROS12, one per sector.

In principle, each wheel is subdivided in an upper part (sectors 1 to 6) that are connected to the ROSs of the TOP crate and a bottom part (sectors 7 to 12) connected to the ROSs of the BOTTOM crate.

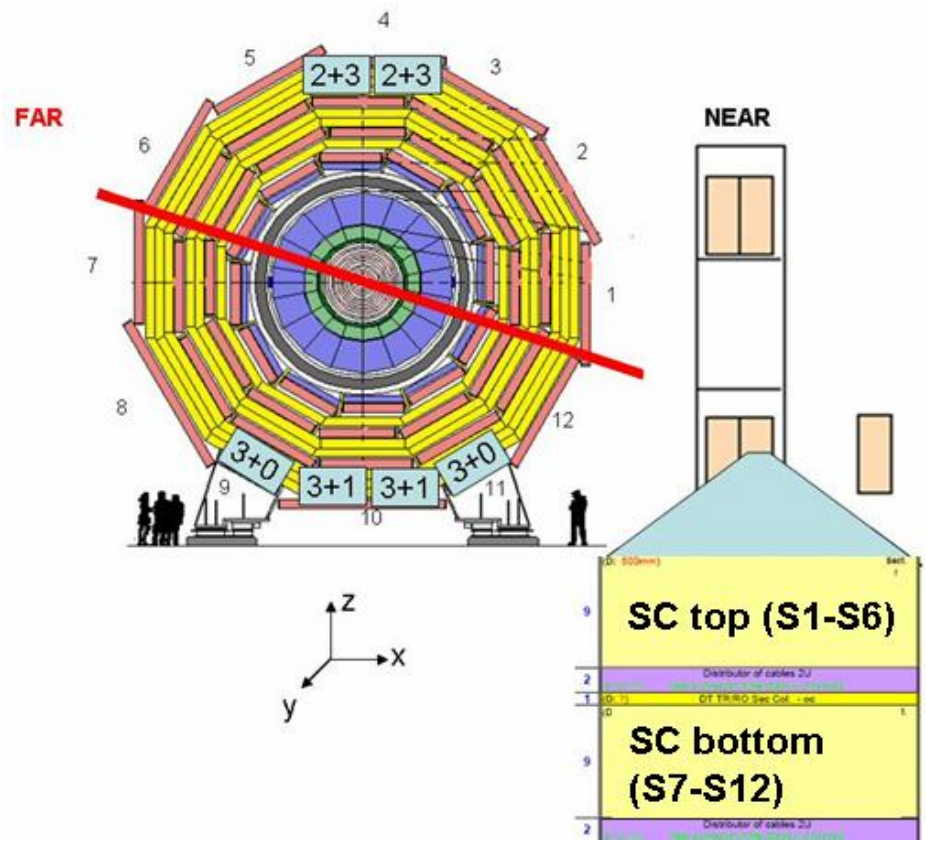

Figure 2: View of the two Sector Collectors crates for one CMS wheel.

Minicrate to Read-Out Server (ROS) links have been distributed in order to minimize the required number of connectors on the ROS while maintaining a unique ROS board format for every sector. The ROS board has been designed with 25 channels to read in average one full sector, and each ROS has 8 RJ-45 connectors with some of its pairs operational according to the following tables:

Connector	Number of links	Cable	Coming from
RJ1	3	MB1-A	MB1 (ROB 0 to 2)
RJ2	3	MB1-B	MB1 (ROB 3* to 5)
RJ3	3	MB2-A	MB2 (ROB 0 to 2)
RJ4	3	MB2-B	MB2 (ROB 3 to 5)
RJ5	4	MB3-A	MB3 (ROB 0 to 3)
RJ6	3	MB3-B	MB3 (ROB 4 to 6)
RJ7	3		Depends on the sector
RJ8	3		Depends on the sector

Note: * ROB 3 of MB1 is a ROB-32 (32 channels instead of 128).

At sectors 1, 2, 3, 5, 6, 7, 8 and 12, connectors RJ7 and RJ8 are related to MB4(ROB 0 to 2) and MB4(ROB 3 to 5) respectively, but as sectors 4 and 10 have two chambers MB4 each, the extra channels have been accommodated in the ROS boards reading sectors 9 and 11 that have fewer channels. A patch panel is attached to the Sector Collector crate to allow interconnection. Final scheme for connectors RJ7 and RJ8 is presented in the following table:

	Con-nector	Number of links	Cables		Coming from
ROS for sectors (1,2,3,5,6,7 8 and 12)	RJ7	3	MB4-A	MB4(s)-1	3 from MB4 (ROB 0 to 2)
	RJ8	3	MB4-B	MB4(s)-2	3 from MB4 (ROB 3 to 5)
ROS 4	RJ7	3	MB4-A	MB4(4)3-2	3 from MB4(4)3 (ROB 2 to 4)
	RJ8	3	MB4-B	MB4(4)5-2	3 from MB4(4)5 (ROB 2 to 4)
ROS 9	RJ7	3	MB4-A	MB4(9)-1	3 from MB4(9) (ROB 0 to 2)
	RJ8	3	MBX	MB4(4)5-1 + MB4(10)9-2	2 from MB4(4)5 (ROB 0 and 1) + 1 from MB4(10)9 (ROB 3)
ROS 10	RJ7	3	MB4-A	MB4(10)11-1	3 from MB4(10)11 (ROB 0 to 2)
	RJ8	3	MB4-B	MB4(10)9-1	3 from MB4(10)9 (ROB 0 to 2)
ROS 11	RJ7	3	MB4-A	MB4(11)-1	3 from MB4(11) (ROB 0 to 2)
	RJ8	3	MBY	MB4(4)3-1 + MB4(10)11-2	2 from MB4(4)3 (ROB 0 and 1) + 1 from MB4(10)11 (ROB 3)

	SECTOR									
ROS Channel	**1,2,3,5,6,7,8,12**		**4**		**9**		**10**		**11**	
0	MB1	ROB 0	MB1	ROB 0	MB1	ROB 0	MB1	ROB 0	MB1	ROB 0
1	MB1	ROB 1	MB1	ROB 1	MB1	ROB 1	MB1	ROB 1	MB1	ROB 1
2	MB1	ROB 2	MB1	ROB 2	MB1	ROB 2	MB1	ROB 2	MB1	ROB 2
3	MB1	ROB 3	MB1	ROB 3	MB1	ROB 3	MB1	ROB 3	MB1	ROB 3
4	MB1	ROB 4	MB1	ROB 4	MB1	ROB 4	MB1	ROB 4	MB1	ROB 4
5	MB1	ROB 5	MB1	ROB 5	MB1	ROB 5	MB1	ROB 5	MB1	ROB 5
6	MB2	ROB 0	MB2	ROB 0	MB2	ROB 0	MB2	ROB 0	MB2	ROB 0
7	MB2	ROB 1	MB2	ROB 1	MB2	ROB 1	MB2	ROB 1	MB2	ROB 1
8	MB2	ROB 2	MB2	ROB 2	MB2	ROB 2	MB2	ROB 2	MB2	ROB 2
9	MB2	ROB 3	MB2	ROB 3	MB2	ROB 3	MB2	ROB 3	MB2	ROB 3
10	MB2	ROB 4	MB2	ROB 4	MB2	ROB 4	MB2	ROB 4	MB2	ROB 4
11	MB2	ROB 5	MB2	ROB 5	MB2	ROB 5	MB2	ROB 5	MB2	ROB 5
12	MB3	ROB 0	MB3	ROB 0	MB3	ROB 0	MB3	ROB 0	MB3	ROB 0
13	MB3	ROB 1	MB3	ROB 1	MB3	ROB 1	MB3	ROB 1	MB3	ROB 1
14	MB3	ROB 2	MB3	ROB 2	MB3	ROB 2	MB3	ROB 2	MB3	ROB 2
15	MB3	ROB 3	MB3	ROB 3	MB3	ROB 3	MB3	ROB 3	MB3	ROB 3
16	MB3	ROB 5	MB3	ROB 5	MB3	ROB 5	MB3	ROB 5	MB3	ROB 5
17	MB3	ROB 6	MB3	ROB 6	MB3	ROB 6	MB3	ROB 6	MB3	ROB 6
18	MB4	ROB 0	MB4-4 (3)	ROB 2	MB4	ROB 0	MB4-10 (11)	ROB 0	MB4	ROB 0
19	MB4	ROB 1	MB4-4 (3)	ROB 3	MB4	ROB 1	MB4-10 (11)	ROB 1	MB4	ROB 1
20	MB4	ROB 2	MB4-4 (3)	ROB 4	MB4	ROB 2	MB4-10 (11)	ROB 2	MB4	ROB 2
21	MB4	ROB 3	MB4-4 (5)	ROB 2	MB4-4 (5)	ROB 0	MB4-10 (9)	ROB 0	MB4-4 (3)	ROB 0
22	MB4	ROB 4	MB4-4 (5)	ROB 3	MB4-4 (5)	ROB 1	MB4-10 (9)	ROB 1	MB4-4 (3)	ROB 1
23	MB4	ROB 5	MB4-4 (5)	ROB 4	MB4-10 (9)	ROB 3	MB4-10 (9)	ROB 2	MB4-10 (11)	ROB 3
24	MB3	ROB 4	MB3	ROB 4	MB3	ROB 4	MB3	ROB 4	MB3	ROB 4
25	SC		SC		SC		SC		SC	

Here, MB4(4)5 stands for Minicrate MB4 from sector 4 that is closest to sector 5, and MB(4)3, the closest to sector 3. Idem for MB4(10)9 and MB4(10)11.

In the following diagram the front panel of the ROS-25 is shown. **Note that connectors are not in consecutive order.**

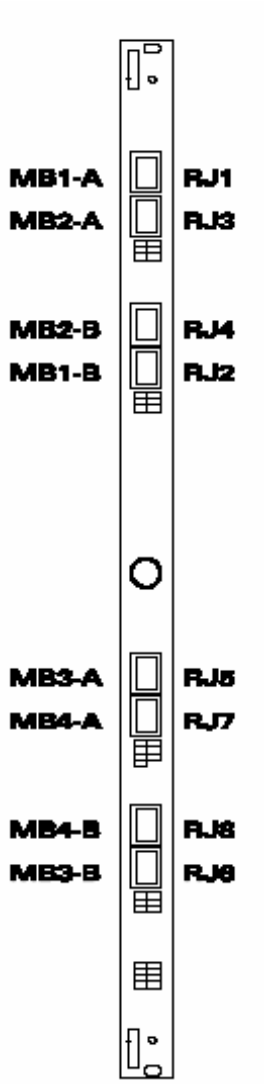

Figure 3: Scheme of the ROS-25 front panel.

POner fotos del patch panel MBX, MBY XXX

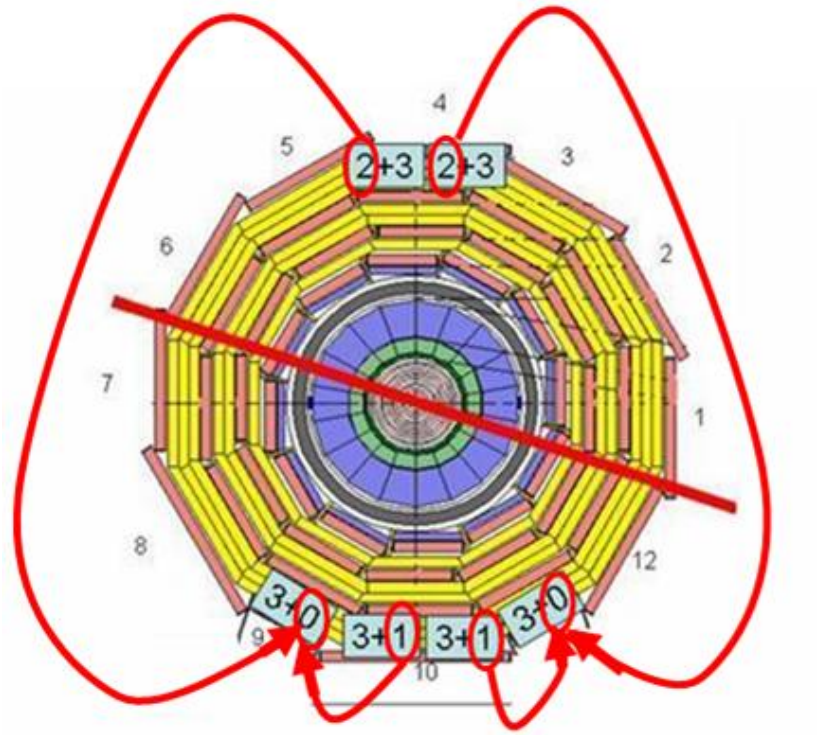

Figure XX: Mapping of ros channels from sector 4 and sector 10 to sector 9 and sector 11.

3 SECTOR COLLECTOR CRATE

The preliminary layout of each crate is presented in figure 4. Inside each crate there will be: 6 ROS boards, 6 Sector Collector boards, a TIM board [5] a 3U VME controller and 3 TTC [3] boards for splitting and fan-out of the TTC optical signal to the Minicrates and also to the Sector Collector crate. And finally, the crate will also include a patch panel for grouping ROB-ROS channels and the connectors for the 5V power supply of the Sector Collector crate.

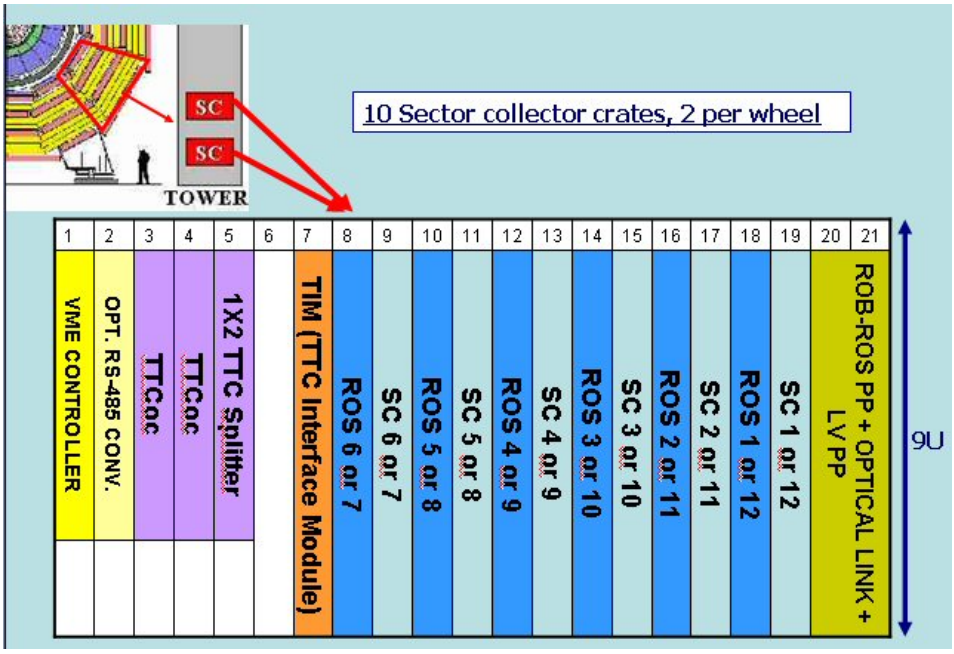

Figure 4: Diagram of the Sector Collector crate and the different boards at each slot.

The TIM module is a 9U board used for receiving the optical TTC signal and retransmitting the decoded information to the ROS and the Sector Collector boards through a 3U and 13 slots backplane located in the bottom part of the crate.

Through the TIM backplane the following TTC signals are retransmitted:

- L1A
- Bunch counter reset
- Event counter reset
- Bunch counter value at the corresponding L1A (12 bits).
- Event counter value at the corresponding L1A (24 bits).
- Other B-Go commands for the Sector Collector board.

It has to be noted that by default the ROS will read the Bunch and Event counter values from the TIM backplane and not from an internal counter. These values are decoded at the TTCrx device at each TIM board.

In order to obtain proper values of these two counters at the ROS and SC, the TTCrx has to be operated in trigger mode “11” (as it is by default), that is, there cannot be two consecutive triggers separated in less than 75 ns, or in other words, the maximum L1A frequency is 13.33MHz. The following picture clarifies this requirement, however, for more information you can have a look at the TTCrx user manual [6].

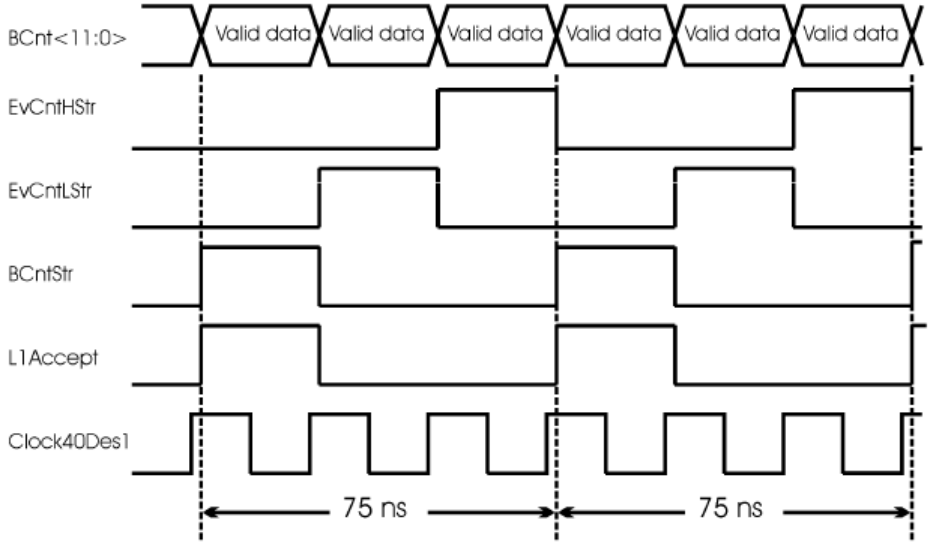

Figure 5: Trigger mode “11” at the TTCrx.

3.1 Base Address

The base address in the Sector Collector crate are arranged in the following order:

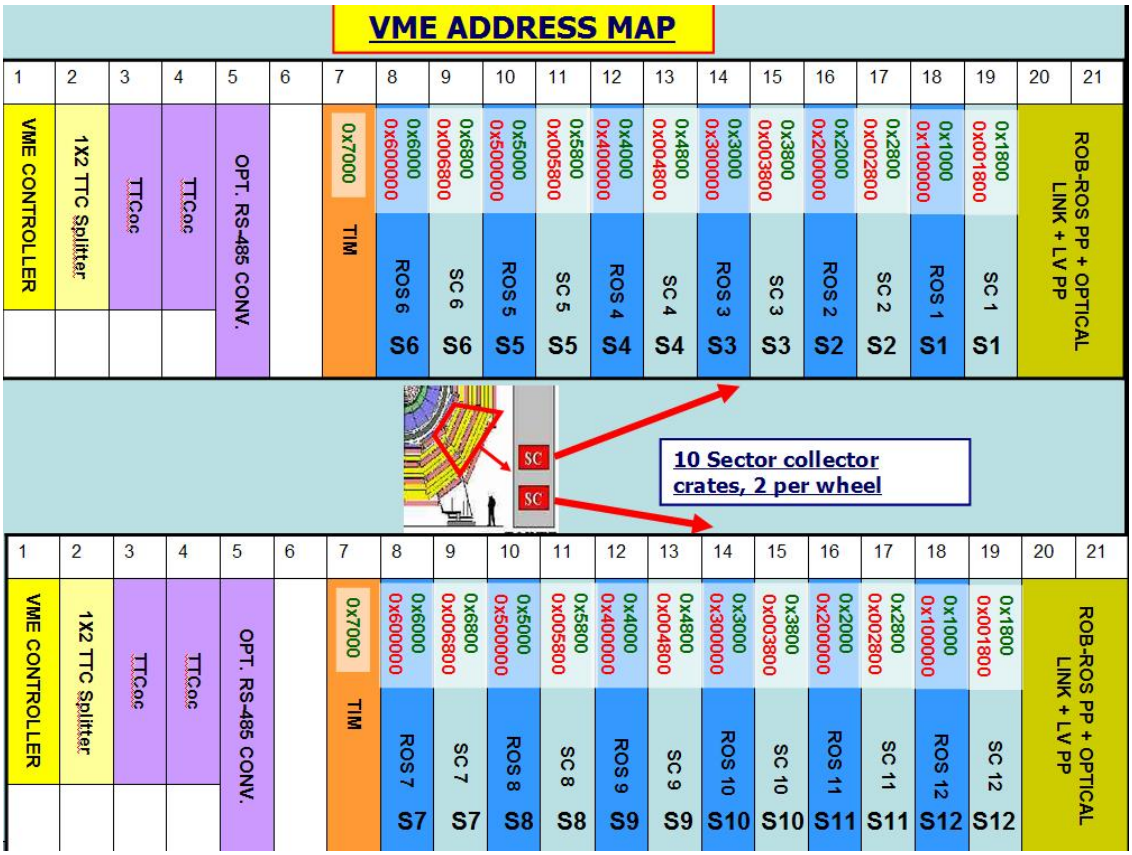

Figure 6: Base address at the Sector Collector crate.

4 OVERVIEW OF THE ROS-25 DESIGN

At the ROS, the 25 channels are grouped in blocks of 6 channels, controlled by an FPGA device that performs the read-out of these channels and checks whether the channels are locked, there are parity errors, etc. Each of these groups of 6 channels is called a CEROS, and there are four of these functional blocks in a ROS as can be seen in figure 2.

There is also a fifth CEROS functional block (CEROS 4) that handles only 1 input channel, number 25th. It is identical to the other four CEROS but only for 1 channel.

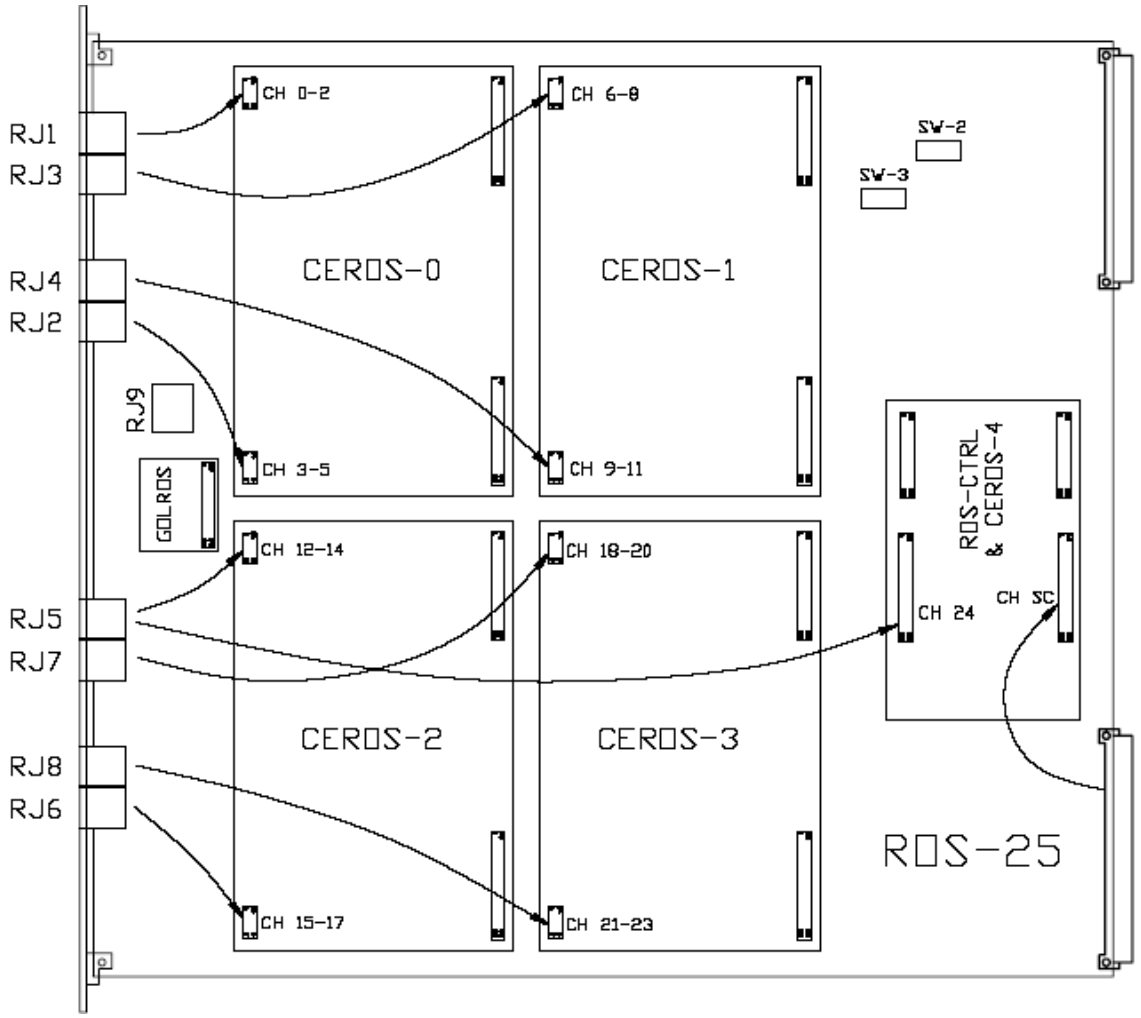

Figure 5: Diagram of the ROS-25 with its main piggy boards.

Another functional module in the ROS is called ROSCTRL. This module contains: first of all, the "Sector Collector channel", and second, the control of the whole read-out functionality.

In certain modes of operation, it may be desired to read the Sector Collector trigger data within the DAQ data flow. Therefore, each Sector Collector board will send, at each event, their

data to its contiguous ROS in the crate, and these data will be treated by the ROS as if it was another input channel, the 26th.

Finally, we can find also the GOLROS module, the last functional block in the ROS which includes the GOL serializer and the VCSEL optical transmitter.

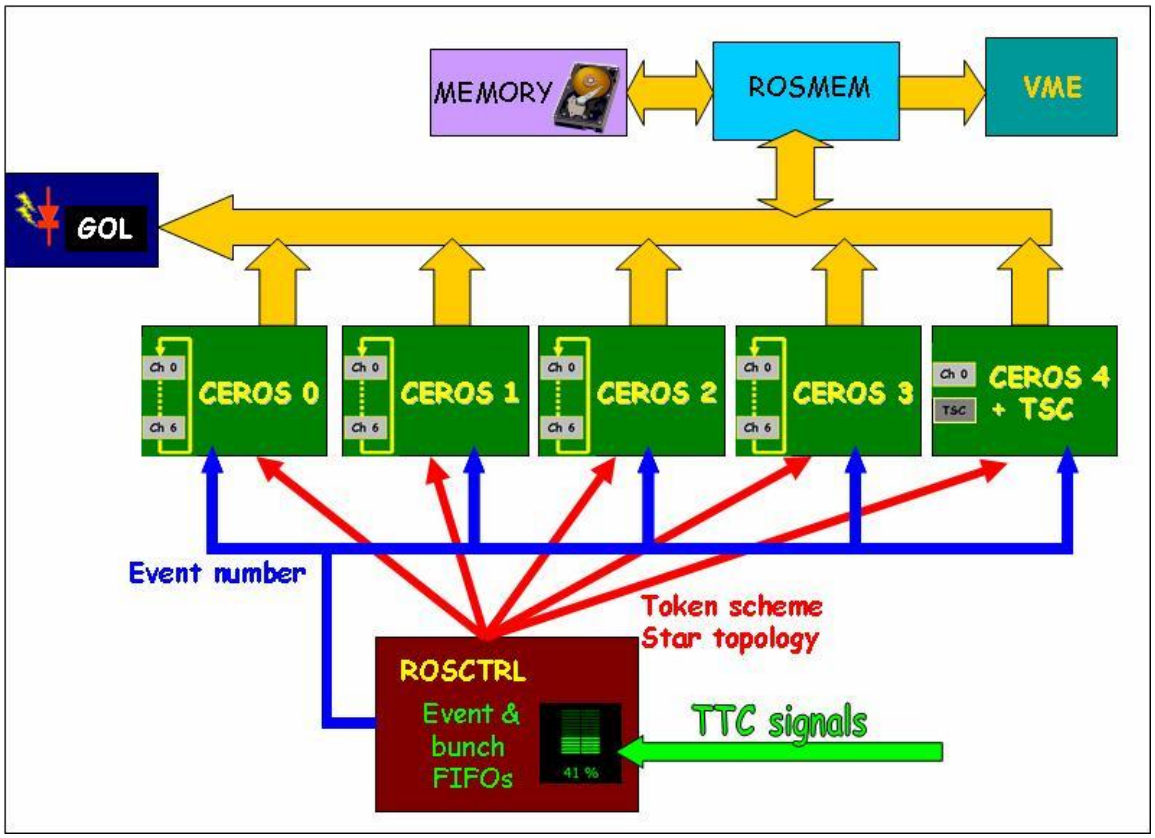

Figure 5: Diagram of the ROS architecture.

Related to how the read-out is performed, the ROS can be programmed in different modes of operation:

- **Normal operation mode:**
  Event and bunch information is received from the TTC system and stored in 255 words FIFOs. Events are processed in parallel in each group of 6 channels (CEROS). Data is sent to a common bus following a token ring scheme for serialization and optical transmission to the DDU through an optical link.

- **Spy mode:**
  Besides sending the data to the DDU, the ROS can store a programmable number of words or of events in a spy memory 512 kBytes long. This memory can be accessed through a VME interface in normal or block transfer mode. This mode of operation can be used in parallel with normal operation mode, it does not interfere.

- **Transmission test mode (GOL_TEST):**
  Through a VME interface, data can be written in the internal ROS memory and then sent through the optical transmitter to the DDU. The number of words sent and also the average bandwidth can be selected.

- **Straight FIFO read-out:**
  This mode of operation has been implemented for debugging purposes, where data are read through VME directly from the input FIFOs. In this way, the format of the data will be the same that comes from the HPTDC, as the ROS is almost transparent in this operation mode.

  These different operation modes are schematically represented in the following figure:

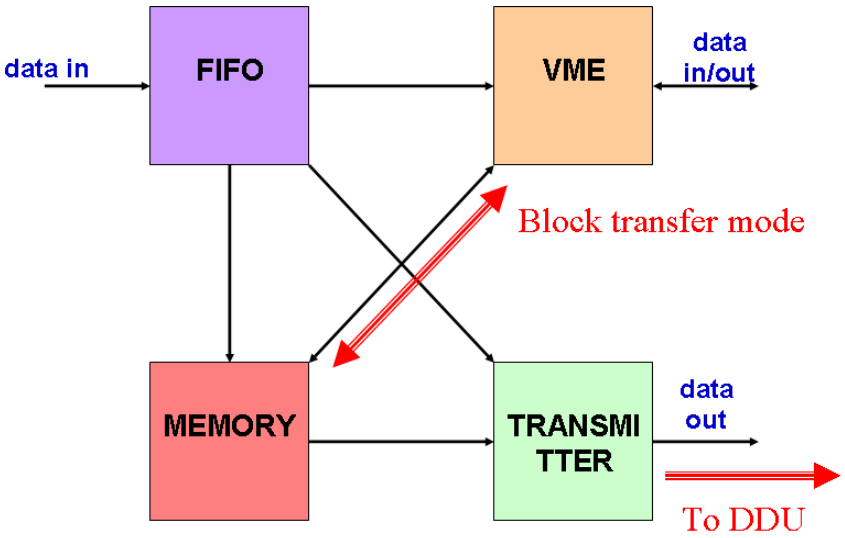

Figure 6: ROS-25 functional diagram.

5 ROS-25 VME INTERFACE

The ROS-25 supports different access modes:

Access type	Data Width	Minimum address space needed	
Short non-privileged A16	Word (16 bits)	1024 words (0x400)	Access to all of the ROS-25 registers
Standard A24 non-privileged	Word (16 bits)	256 kwords (0x40000)	Access to the memory.
Standard A24 standard non-privileged block transfer	Word (16 bits)	256 kwords (0x40000)	Access to the memory.

The A16 base address is selected with switch SW3, (A15-A10), and the A24 address is selected with switch SW2, (A23–A20). The address mapping for the registers of the different functional blocks is what follows:

A16 Base Address (A15 – A10)	Functional block
Base Address + 0x00	CEROS0
Base Address + 0x80	CEROS1
Base Address + 0x100	CEROS2
Base Address + 0x180	CEROS3
Base Address + 0x200	CEROS4
Base Address + 0x280	ROSCTRL
Base Address + 0x300	MEMCTRL
Base Address + 0x380	ROSVME

5.1 Memory access : A24 access, word width

It can be standard or non-privileged block data transfer.

Address from 0x00000 to 0x7FFFE (256kwords = 262144 words)

0-15	Memory Data	R/W

5.2 Registers access: A16 access, word width.

5.2.1 ROSVME

All the registers from ROSVME are not reset by a global reset but by a local reset, except for the registers belonging to the PCA9564 device.

Control y status (ROSVME + 0x00) = 0x380

Default value = 0x7D
Reset by a hard reset.

bits	description	acc	
0	ROS waiting	R	1 = ROS has finished processing an event.
1	Memory Done	R	1 = programmed limit achieved
2	CEROS 0 FPGA's programmed	R	1 = OK programmed
3	CEROS 1 FPGA programmed	R	1 = OK programmed
4	CEROS 2 FPGA programmed	R	1 = OK programmed
5	CEROS 3 FPGA programmed	R	1 = OK programmed
6	ROSCTRL FPGA programmed	R	1 = OK programmed
7	'0'	R	
8	Enable EVCNT_reset to perform a soft reset.	R/W	
9	Select GOL clock	R/W	0 = ckdesv1, 1 = ckdesv2
10	Select ROS-25 clock	R/W	0 = ckdesv1, 1 = ckdesv2
11	Load PAF values in all the FIFOs	W	
12	Partial CEROS FIFO reset (PRS)	W	Will also be executed with a soft reset.
13	Master CEROS FIFO reset (MRS)	W	Will also be executed with a hard reset.
14	Hard reset	W	
15	Soft reset	W	

A VME sys-reset will force also a hard reset and will also reprogram the FPGAs (by hardware).

Bits 9 and 10 select among the two output clocks from the TTCrx device with their corresponding programmed de-skew. As the output of the ckdesv2 signal is disabled at the TTCrx device by default and for the ROS-25 prototypes it is not recommended to use ckdesv2, we do not recommend writing a 1 in any of those two bits. (The last does not apply to the ROS-25 prototype at Torino).

Soft reset is executed by:

- Writing 0x8000 in register ROSVME+0x00.
- When receiving an Event Reset signal from the TTC system if it is enabled in bit 8 of ROSVME+0x00.
- Whenever a hard reset is executed.

Hard reset is executed by:

- Writing 0x4000 in register ROSVME+0x00.
- When a sysreset is received from the VME controller.

RESYNC (TTC commands)

ROS does not react to the RESYNC command. Instead, it reacts to the Event counter reset command and performs a soft reset (if the ROS has been configured in that way, bit 8 of ROSVME + 0x00).

SPAF / SFF (ROSVME + 0x04) = 0x384

Default value: 0x00
Reset by a soft reset

bits	description	acc	
0	Ceros 0 SPAF	R	1 = Almost Full flag active in any of the FIFOs of each CEROS.
1	Ceros 1 SPAF	R	1 = Almost Full flag active in any of the FIFOs of each CEROS
2	Ceros 2 SPAF	R	1 = Almost Full flag active in any of the FIFOs of each CEROS
3	Ceros 3 SPAF	R	1 = Almost Full flag active in any of the FIFOs of each CEROS
4	'0'	R	
5	Ceros 0 SFF	R	1 = Full flag active in any of the FIFOs of each of the CEROS.
6	Ceros 1 SFF	R	1 = Full flag active in any of the FIFOs of each of the CEROS.
7	Ceros 2 SFF	R	1 = Full flag active in any of the FIFOs of each of the CEROS.
8	Ceros 3 SFF	R	1 = Full flag active in any of the FIFOs of each of the CEROS.
9-15	'0'	R	

CEROS 4 does not send SPAF and SFF to ROSVME, has to be checked directly on its registers. Accordingly, no interruption is possible on SPAF or SFF for CEROS 4 (channel 24).

Interruptions (ROSVME + 0x06) = 0x386

Default = 0x 20
Reset by a hard reset.

bits	Description	acc	
0	enable SPAF interrupt	R/W	If any of the FIFOs signals the almost full flag (PAF), an interruption will take place. (Except channel 24)
1	enable SFF interrupt	R/W	If any of the FIFOs gets full at any time, an interruption will take place. (Except channel 24)
2	enable memory done interrupt (rising edge)	R/W	An interruption will occur when the ROS has achieved the programmed condition (number of words/events to be transmitted/stored on memory).
3	enable ROS waiting interrupt (rising edge)	R/W	An interruption will occur when the ROS finishes processing an event. To be used only in normal or spy mode.
4	interrupt requested	R	= 1 An interruption from the ROS has

			occurred.
5-7	interrupt level	R/W	
8-15	interrupt vector	R/W	

FPGA Control (ROSVME + 0x08) = 0x388

Default value = 0x1000
Default value = 0x9000 ???

Reset by a hard reset.

bits	description	acc	
0	CEROS 0 INIT signal	R/W	If the INIT bit is set to 1, whenever that FPGA is reprogrammed it will be standing in erase mode until the INIT bit is released.
1	CEROS 1 INIT signal	R/W	
2	CEROS 2 INIT signal	R/W	
3	CEROS 3 INIT signal	R/W	
4	ROSCTRL INIT signal	R/W	
5	Reprogram CEROS 0 FPGAs	W	When writing a 1 here, CEROS 0 FPGAs is reprogrammed
6	Reprogram CEROS 1 FPGAs	W	1 => CEROS 1 reprogrammed
7	Reprogram CEROS 2 FPGAs	W	1 => CEROS 2 reprogrammed
8	Reprogram CEROS 3 FPGAs	W	1 => CEROS 3 reprogrammed
9	Reprogram ROSCTRL FPGAs	W	1 => ROSCTRL reprogrammed
10-12	Select clock frequency for loading FPGAs from their program memories	R/W	Default 20 MHz => 4 ms
13	Enables reprogramming FPGAs with an event reset signal.	R/W	
14	Enables reprogramming FPGAs with a soft reset signal.	R/W	
15	Enables reprogramming FPGAs with a TTC HARDRESET	R/W	Set default as 1

Note: FPGA load clock frequency:

- 000 – 1,25 MHz
- 001 – 2.5 MHz
- 010 – 5 MHz
- 011 – 10 MHz
- **100 – 20 MHz (default) (Time to load 4 ms??)**
- Others => 1,25 MHz **(Time to load 63 ms??)**

JTAG Control (ROSVME + 0x0A) = 0x38A

Default value = 0x7
Reset by a hard reset.

bits	description	acc
0-2	Selection of the device to be configured through connector J1	R/W

0 Configure CEROS 0
1 Configure CEROS 1
2 Configure CEROS 2
3 Configure CEROS 3
4 Configure ROSCTRL
5 Configure ROSMEM
6 Configure devices through VME (The device to configure has to be selected afterwards in register ROSVME+0x0C).
7 Device selected from corresponding position of switch SW1.

JTAG Register 1 (ROSVME + 0x0C) = 0x38C

Default value = 0x0
Reset by a hard reset.

bits	description	acc
0	Enables JTAG access to CEROS 0 FLASH	R/W
1	Enables JTAG access to CEROS 1 FLASH	R/W
2	Enables JTAG access to CEROS 2 FLASH	R/W
3	Enables JTAG access to CEROS 3 FLASH	R/W
4	Enables JTAG access to ROSCTRL FLASH	R/W
5	Enables JTAG access to ROSMEM	R/W
6	flash_tck	R/W
7	flash_tms	R/W
8	flash_tdi	R/W
9	flash_tdo of CEROS 0	R
10	Flash_tdo of CEROS 1	R
11	Flash_tdo of CEROS 2	R
12	Flash_tdo of CEROS 3	R
13	Flash_tdo of ROSCTRL	R
14	Flash_tdo of ROSMEM	R

JTAG TDI Register 2 (ROSVME + 0x0E) = 0x38E

Default value = 0x0
Reset by a hard reset.

bits	description	acc
7-0	Flash TDI (7 downto 0)	R/W
8	Flash TMS	R/W
12-9	Bits to send (max 8)	R/W

The state machine to send the TDI bits is activated as soon as anything is written in this register.

JTAG TDO Data (ROSVME + 0x10) = 0x390

Default value = 0x0
Reset by a hard reset.

bits	description	acc
0-7	Sequence of bits received (TDO) (bit 0 last received)	R
8	Finished	

I2C & 1-wire & GOL & QPLL (ROSVME + 0x12) = 0x392

Default value = 0xE8
Reset by a hard reset.

bits	description	acc	
0	Enable I2C access to GOL	R/W	
1	Enable I2C access to I,V, T sensors	R/W	
2	GOL power off	R/W	After a hard reset the GOL will be switched OFF.
3	GOL ready	R	=1 ok.
4	QPLL error registered	R	A SEU error occurred at the QPLL.
5	QPLL locked	R	=1 ok.
6	QPLL unlocked registered	R	=1 at some point the QPLL has unlocked.
7	GOL not ready registered	R/W	=1 at some point the GOL was not ready.
8	QPLL reset	W	
9	Clock selected	R	=0 Clock is being received from the backplane. (Normal operation mode) =1 Clock is coming from the internal ROS 40 MHz crystal.
10	Clock selected_reg	R/W	=1, at some point the clock has come from the internal ROS 40 MHz crystal.
11	GOL reset	W	
12	I2C reset	W	=1 a reset of the PCA9564 is generate

Bits 0 and 1 can not be enabled at the same time, so if ever a 1 is written on both at the same time, only the access to the I, V, T sensors will be enabled.

I2C reset is active low and needs to be low at least 10 ns (guaranteed)

I am changing completely this register, after a reset the GOL does not switch OFF

Note that:

QPLL is reset:

- Writing a 1 in bit 8 of ROSVME+0x12.
- With a hard reset.

GOL is reset:

- Writing a 1 in bit 11 of ROSVME+0x12.
- With a hard reset.

I2C (PCA9564) is reset:

- Writing a 1 in bit 12 of ROSVME+0x12.
- With a hard reset.

PCA_STATUS (ROSVME + 0x20) = 0x3A0

bits	description	acc	default
0-7	Status	R	0xF8
0-7	Time-out	W	0xFF

PCA_DATA (ROSVME + 0x22) = 0x3A2

Default = 0x00

bits	description	acc
0-7	Data	R/W

PCA_ADDRESS (ROSVME + 0x24) = 0x3A4

Default = 0x00

bits	description	acc
0-7	Own address	R/W

PCA_CONTROL (ROSVME + 0x26) = 0x3A6

Default = 0x00

bits	description	acc	Description
7	AA	R/W	Assert acknowledge flag
6	ENSIO	R/W	SIO enable bit
5	STA	R/W	Start flag
4	STO	R/W	Stop flag
3	SI	R/W	Serial interrupt flag
2-0	CR	R/W	Serial clock rate

CR: Serial clock frequency

000	330 kHz
001	288 kHz
010	217 kHz
011	146 kHz
100	88 kHz
101	59 kHz
110	44 kHz

111	36 kHz

The I2C protocol is reset with a hard reset and by writing a 1 in bit 12 of register “I2C & 1-wire & GOL & QPLL (ROSVME + 0x12)”

5.2.2 ROSMEM

Control y status (ROSMEM + 0x00) = 0x300

Default value = 0x00
Reset by a hard reset.

bits	description	acc
0	Enables transfer from memory to GOL. Mode GOL_TEST. If only this bit is set to 1, an unlimited transfer takes places. It can be stopped again by writing a 0 into this bit.	R/W
1	Enables storing FIFOs data in ROS memory (SPY MODE). Any of bits 2, 3 or 4 should also be selected. The storage can also be forced to stop by writing a 0 again into this bit, in such a case, if limit by number of events is selected, the ROS will stop to write on the memory as soon as the actual event is completed.	R/W
2	Limits transfer by number of words. For GOL_TEST or SPY MODE.	R/W
3	Limits transfer by number of events. Only for SPY MODE.	R/W
4	Enables transfer until memory full. For mode GOL_TEST or SPY MODE. 262143 words will be sent or written into the memory.	R/W
5	Enables repeat cycles of number of words for sending data to the transmitter. Only for mode GOL_TEST.	R/W
6	Selects random transmission enable for GOL_TEST mode of operation.	R/W
7-10	Enables corresponding LFSR register for random transmission enable. Only for mode GOL_TEST.	R/W

The transmitter enable signal that loads the 16 bit words data into the GOL transmitter is generated by default in GOL_TEST mode as a 20 MHz clock, obtaining therefore a bandwidth of 320 Mbps.

If bit 6 is set to 1, then, a random transmitter enable signal can be chosen. This random signal is obtained as the output of some pseudo-random shift registers (LFSR). Bits 7 to 10 enable each a LFSR register, and the transmitter enable signal is obtained as the logical AND of each of the enabled LFSR.

As these LFSR run at 40 MHz, the average frequency is also 20 MHz. By enabling more LFSRs the average bandwidth can be reduced to something more similar to the expected value during normal ROS operation mode: (~100 Mbps)

1 LFSR enabled: 20 MHz => 320 Mbps
2 LFSR enabled: 10 MHz => 160 Mbps
3 LFSR enabled: 5 MHz => 80 Mbps
4 LFSR enabled: 2,5 MHz => 40 Mbps

Memory pointer low (ROSMEM + 0x02) = 0x302

Default value = 0x00
Reset by a hard reset.

bits	description	acc
0-15	Memory address pointer (bits 0-15)	R/W

Memory pointer high (ROSMEM + 0x04) = 0x304

Default value = 0x00
Reset by a hard reset.

bits	Description	acc
0-1	Memory address pointer (bits 16-17)	R/W
2	Resets the memory pointer	W

The memory pointer gives the number of 16 bit words stored in the memory.

Max word (16 bits) count low (ROSMEM + 0x06) = 0x306

Default value = 0x00
Reset by a hard reset.

bits	Description	acc
0-15	Maximum number of words (bits 0-15)	R/W

Max word (16 bits) count high (ROSMEM + 0x08) = 0x308

Default value = 0x00
Reset by a hard reset.

bits	Description	acc
0-1	Maximum number of 16 bits words (bits 16-17)	R/W
2	Resets max word count register	W

Max event count (ROSMEM + 0x0A) = 0x30A

Default value = 0x00
Reset by a hard reset.

bits	Description	acc
0-15	Maximum number of events	R/W

Cycle count (ROSMEM + 0x0C) = 0x30C

Default value = 0x00
Reset by a hard reset.

bits	description	acc
0-15	Number of cycles to repeat the transmission	R/W

If number of cycles is set to 0, then 65536 cycles (0x10000) will be performed.

5.2.3 CEROS 0-4

CEROSX is replaced by the base address of the corresponding CEROS. Note that CEROS 4 only has one channel (related information is located in the least significant bit).

LOCK / MASK (CEROSX + 0x00) = 0x0 , 0x80, 0x100, 0x180, 0x200

Bits	description	acc		Signal that resets
0-5	Channel UNLOCK	R	1 = channel is unlocked	Soft reset
6-11	MASK Channel	R/W	1 = channel masked	Hard reset
12-14	CEROS identification	R	0 for ceros 0, 1 for ceros 1, 2 for ceros 2, 3 for ceros 3, 4 for ceros 4	

DISABLE REGISTER (CEROSX + 0x02) = 0x2, 0x82, 0x102, 0x182, 0x202

Default value = 0x90 (No blocking if EVID mis, no error PAF words by default)
Reset by a hard reset.

Bits	Description	Acc	Default
0	Disable MAXWORDS to block channel	R/W	0
1	Disable HAS UNLOCK, LOCK or FIFO FULL to block channel	R/W	0
2	Disable TIMED OUT to block channel	R/W	0
3	Enable to read full event even if Fifo Full	R/W	0
4	Disable send PAF warning word within the data.	R/W	1
5	Disable send EVID misalignment error word within the data.	R/W	0
6	Enable send HPTDC data although there are no hits.	R/W	0
7	Disable EVID misalignment to block channel	R/W	1
8	Disable send debug error words	R/W	0
9	??? nothing?		
10	Channel 0 blocked resynch independent	R	
11	Channel 1 blocked resynch independent	R	
12	Channel 2 blocked resynch independent	R	
13	Channel 3 blocked resynch independent	R	
14	Channel 4 blocked resynch independent	R	
15	Channel 5 blocked resynch independent	R	

If for any reason the ROS blocks automatically one of the channels, it will be signalled with a 1 in the Channel blocked field. A channel will appear as blocked either because the user has masked it by writing in register LOCK/MASK or due to any of the following malfunctions:

- The channel is unlocked or has unlock at any time or its fifo has been full and the option “Disable HAS UNLOCK, LOCK or FIFO FULL to block channel” was set to 0.
- The channel has timed out and the option “Disable TIMED OUT to block channel” was set to 0.
- More than the programmed number of consecutive words (register ceros+0x18) have been read out from that channel without finding a ROB trailer and the option “Disable MAXWORDS to block channel” was set to 0.

- There has been an Event ID misalignment in that channel and the option "Disable EVID misalignment to block channel" was set to 0.

Also, if "Enable to read full event even if Fifo Full" is set to 0, whenever the fifo is full, it will be blocked on that event, and therefore, whatever was I that fifo will not be read. If that bit is set to 1, it will try to read the contents of the fifo (but it will be blocked either way unless "Disable HAS UNLOCK, LOCK or FIFO FULL to block channel" is set to 0), until the fifo is emptied and then we will get a timeout.

TIMEDOUT / HASUNLOCK (CEROSX + 0x04) = 0x4, 0x84, 0x104, 0x184, 0x204

Reset by a soft reset.

bits	Description	acc
0-5	Channel has TIMED OUT	R/W
6-11	Channel HAS UNLOCK	R/W

There is only one reasons why a channel can signal a timeout:

- The FIFO is empty longer than the timeout value programmed for that group of 6 channels (register TIMEOUT VALUE). Therefore, the programmed timeout should be long enough to cope with the different latency of the L1A signal between the Minicrates and the ROS and include also the propagation time between the cooper links from Minicrates to ROS.

PAF (CEROSX + 0x06) = 0x6, 0x86, 0x106, 0x186, 0x206

Reset by a soft reset.

bits	Description	acc	
0-5	FIFO's PAF	R	= 1 an Almost Full condition has been achieved in the FIFO of the corresponding channel.
6-11	FIFO's PAF REGISTERED	R/W	Registered value of the previous.

EF (CEROSX + 0x08) = 0x8, 0x88, 0x108, 0x188, 0x208

Reset by a soft reset.

bits	description	acc	
0-5	FIFO's EF	R	1 = FIFO is empty
6-11	Event ID misalignment error	R/W	1 = that channel had an event ID misalignment error.

FF (CEROSX + 0x0A) = 0xA, 0x8A, 0x10A, 0x18A, 0x20A

Reset by a soft reset.

bits	description	acc	
0-5	Maxwords reached	R	1 = The maximum number of words in that channel has been received and no ROB trailer has been found.
6-	FIFO's FF	R/W	1 = FIFO has been full at any time.

11	REGISTERED		

PAF VALUE (CEROSX + 0x0C) = 0xC, 0x8C, 0x10C, 0x18C, 0x20C

Default value = 0xFF
Reset by a hard reset.

bits	description	acc	
0-10	FIFO's PAF VALUE	R/W	When the number of empty 16 bits words in a FIFO is smaller than this value, the FIFO will set to 1 the PAF flag. This value is common all channels in a CEROS.
11	RECEIVERS OFF	R/W	= 1 the 6 channels will turn off their receivers, so no data will be received.

The 2kwords input FIFO for each channel has a flag (PAF flag) to signal that the number of empty positions at the FIFO is smaller than a programmed limit, the PAF value.

By default, the PAF value at the FIFOs after a Master Reset (MRS) is 15, that is, when the number of words in the FIFO is larger than 2049-15 = 2034, the PAF flag will be set to 1.

In order to program a new PAF value, it is necessary to write the desired PAF value in this register (at each CEROS) and then write a 1 in bit 11 of register ROSVME+0x00 to download the new value into the FIFOs. During this task, the channels will be unlocked, so before taking data again, the TIMEDOUT/HASUNLOCK register should be erased.

If a Master CEROS FIFO reset (MRS) is performed, the programmed PAF value in the FIFOs will be erased. To empty the data in a FIFO without erasing the programmed PAF value, a Partial CEROS FIFO reset (PRS) should be used instead.

FIFO WORD PARITY (CEROSX + 0x0E) = 0xE, 0x8E, 0x10E, 0x18E, 0x20E

Reset by a hard reset.

bits	description	acc	
0-15	FIFO WORD PARITY	R/W	= 1 a parity error has been detected in a word. The position of that word in the data stream is the same as the corresponding position of the parity bit in this register.

This is a shift register where it is stored the parity errors of the 16 bits words read from the FIFO, starting from the least significant bit.

FIFO BYTE PARITY 0 (CEROSX + 0x10) = 0x10, 0x90, 0x110, 0x190, 0x210

Reset by a hard reset.

bits	description	acc

0-15	FIFO BYTE PARITY bits 0-15	R/W

FIFO BYTE PARITY 1 (CEROSX + 0x12) = 0x12, 0x92, 0x112, 0x192, 0x212

Reset by a hard reset.

bits	description	acc
0-15	FIFO BYTE PARITY bits 16-31	R/W

In these two registers, the actual parity and not the parity error is shifted starting by the least significant bit. In this case, each bit corresponds to the parity of a byte and not of a 16 bits word.

Register BYTE PARITY 0 and 1 have been removed from ceros 4 (rosctrl).

FIFO DISPARITY COUNTER (CEROSX + 0x14) = 0x14, 0x94, 0x114, 0x194, 0x214

Default value = 0x0
Reset by a hard reset.

bits	description	acc
0-15	FIFO DISPARITY COUNTER	R/W

Each time a parity error is found in any of the channels of a CEROS, this counter will be incremented. (Warning, this counter may overflow).

I change it so that if bit 15 =1 it does not move ahead, therefore, maximum value is 8000 and it does not overflow.

TIMEOUT VALUE(CEROSX + 0x16) = 0x16, 0x96, 0x116, 0x196, 0x216

Default value = **0x80** (3.2 µs)
OLD Default value = 0xFF0 (102 µs)
Reset by a hard reset.

bits	description	acc	
0-11	TIME OUT VALUE for all channels of this CEROS	R/W	Number of clock cycles before timeout.

This value corresponds to the number of 40 MHz clock cycles that the ROS will wait when it is reading a channel but its FIFO is empty.

MAXWORDS LIMIT (CEROSX + 0x18) = 0x18, 0x98, 0x118, 0x198, 0x218

Default value = **0x25** (maximum by default, 296 words-32bits)
OLD Default value = 0xFF (maximum by default, 2040 words-32bits)
Reset by a hard reset.

bits	Description	acc	
0-7	Maximum number of blocks of 8 32-bit words per channel to be read.	R/W	

In this register you can program how many multiples of 8 words (32 bit) per ROB channel you want to read. It does not take into account headers and trailers, therefore, it only limits the number of hits or error words.

The minimum programmed number is 8 words, and the maximum is 4095 words.

It might be important to set a limit to the maximum number of ROBs in order to avoid a situation in which it is impossible to find the ROB trailer and the ROS gets stuck reading nonsense data (for example a link that is faulty and is sending nonsense data).

FIFO PAF COUNTER 0-5 (CEROSX + 0x20-2A) = 0x20, 0xA0, 0x120, 0x1A0, 0x220

Default value = 0x0.
Reset by a soft reset.

bits	description	acc
0-15	FIFO 0-5 PAF counter	R/W

It counts the number of times that the programmed almost full limit has been achieved in a particular channel of that CEROS.

FIFO DATA 0-5 (CEROSX + 0x30-3A) = 0x30, 0xB0, 0x130, 0x1B0, 0x230

bits	description	acc
0-15	FIFO 0-5 data	R

TO BE USED ONLY FOR DEBUGING.

By reading at this register, the data from the corresponding channel is taken out from the input FIFO, that is, once read, **it cannot be read again**. When all the data have been read, the Empty FIFO flag will be signalled and the last word read will remain at the FIFO output, so the same value will be read again in following accesses.

Note that data read from this register has the HPTDC data format, and therefore, there is no indication of the number of channel that is being read.

PAE/PAF PROGRAMMED 0-5 (CEROSX + 0x40-4A) = 0x40, 0xC0, 0x140, 0x1C0, 0x240

bits	description	acc
0-10	FIFO 0-5 PAE/PAF programmed	R

The PAF value programmed at each FIFO can be read from these registers.

This register **should only be accessed during configuration, not during data acquisition,** otherwise data at the FIFOs can be corrupted.

TTS (CEROSX + 0x50) = 0x50, 0xD0, 0x150, 0x1D0, 0x250

Default value = 0x1D
Reset by a hard reset.

bits	description	acc	Default
0	Resynch if timeout	R/W	1
1	Resynch if event ID misalignment	R/W	0
2	Warning overflow if PAF	R/W	1
3	Resynch if Fifo Full	R/W	1
4	Resynch if max number of words reached	R/W	1

When setting these bits to 1, you enable to set a flag bit in the error words that the ROS sent (see later). This bit will be processed by the DDU and will force the TTS transitions in the DDU TTS state machine.

ERROR Register 1, not reset by Resynch (CEROSX + 0x52) = 0x52, 0Xd2, 0x152, 0x1D2, 0x252

Default value = 0x0
Reset by a hard reset.

bits	description	acc
5 – 0	Hasunlock (not reset by resynch)	R/W
11 - 6	Timedout (not reset by resynch)	R/W

ERROR Register 2, not reset by Resynch (CEROSX + 0x54) = 0x54, 0xD4, 0x154, 0x1D4, 0x254

Default value = 0x0
Reset by a hard reset.

bits	description	acc
5 - 0	Event ID misalignment (not reset by resynch)	R/W
11 – 6	Fifo full (not reset by resynch)	R/W

ERROR Register 3, not reset by Resynch (CEROSX + 0x56) = 0x56, 0xD6, 0x156, 0x1D6, 0x256

Default value = 0x0
Reset by a hard reset.

Bits	description	acc
5 – 0	Maxwords reached (not reset by resynch)	R/W
11 - 6	PAF (not reset by resynch)	R/W

5.2.4 ROSCTRL (0x280)

CEROS or SC TIMED OUT (ROSCTRL + 0x00) = 0x280

Default value = 0x00
Reset by a soft reset.

bits	description	acc
0-4	CEROS timed out	R/W
5	SECTOR COLLECTOR channel has timed out	R/W
6	SECTOR COLLECTOR channel FIFO full registered.	R/W
7	Bunch ID FIFO full registered.	R/W
8	Event ID HIGH FIFO full registered.	R/W
9	Event ID LOW FIFO full registered.	R/W
10		
11		
12		
13		
14		
15	TXENA_PAR. Set to one if the number of 16 bit words transmitted is odd. Latched.	R/W

The Sector Collector channel is not blocked if at any time its FIFO is full, but some words may be lost. At the moment, the Sector Collector FIFO is 511 words (16 bits) deep, so it should be large enough to cope with the data received from the Sector Collector for 1 event.

MASKS (ROSCTRL + 0x02) = 0x282

New Default value = 0x5420 (I allow CEROS timeout to mask the ceros)
Default value = 0x5460 (I remove orbit counter by default)
OLD Default value = 0x5C60 (before 0x5D40)
Reset by a hard reset.

bits	description	acc
0	Mask CEROS 0	R/W
1	Mask CEROS 1	R/W
2	Mask CEROS 2	R/W
3	Mask CEROS 3	R/W
4	Mask CEROS 4	R/W
5	Enable SECTOR COLLECTOR channel	R/W
6	Disable TIMED OUT to mask CEROS or SECTOR COLLECTOR channel	R/W
7	Enable reception of AUTOL1A trigger at ROS	R/W
8	Disable reception of TTC L1A trigger from TIM module.	R/W
9	Select ROS internal Event ID counter	R/W
10	Enable send BUNCH COUNTER debugging word within the data flow.	R/W
11	Enable send BUNCH RESET COUNTER debugging word within the data flow.	R/W
12	Enable send L1A Warning overflow resynch bit in the data	R/W
13	Read Internal SECTOR COLLECTOR FIFO (to be used for debugging)	R/W
14	Resynch if Ceros has timedout	R/W

15	Noise mask	R/W

Note that the TTC L1A is disabled by default at a reset to allow proper configuration of the ROS although the TTC system is sending L1As.NOT ANYMORE!!!!!

The bit number 13, for reading internal Sector Collector FIFO should be set only for debugging purposes. If it is set, the ROS_READY-TRIGGER_STROBE handshake will not take place.

Bit number 9, "Select local Event ID counter" should be used either for debugging purposes when there is no TTC or TIM boards present, or when the L1A comes from the Sector Collector board (AutoL1A). In such a case, L1As from the TIM board should be disabled (bit 8 to 0).

Bits 12 and 14 are used to flag the corresponding bit in the data that will be processed by the DDU in order to modify the status of its TTS state machine.

TIMEOUT VALUE (ROSCTRL + 0x04) = 0x284

Default value = 0xFFF (102,4 µs)
Reset by a hard reset.

bits	Description	acc
0-11	TIME OUT VALUE for ~~CEROS~~ ~~and~~ SECTOR COLLECTOR channel The real time is = (this value x 2) clock cycles	R/W
12	Disable send ROS general status word	R/W

For the Sector Collector channel, this value represents the time since the ROS_READY signal was set to 1 until a timeout is given because there has been no TRG_STROBE signal from the Sector Collector board.

For the CEROS module, this value should be larger than the maximum number of cycles needed for processing one event in one channel (0x190 ~10 µs).

The programmed value should match the larger of these two timeouts.

New firmware has a fixed value of 0xFFF for the CEROS. This register only applies to the Sector Collector channel.

BUNCH NUMBER (ROSCTRL + 0x06) = 0x286

bits	description	acc	
0-11	Read last BUNCH NUMBER	R	
0-11	Write BUNCH NUMBER in FIFO	W	Should be used only for ROS debugging.

EVENT LOW NUMBER (ROSCTRL + 0x08) = 0x288

bits	description	acc	

0-11	Read last EVENT LOW NUMBER	R	
0-11	Write EVENT LOW NUMBER in FIFO	W	Should be used only for ROS debugging.

EVENT HIGH NUMBER (ROSCTRL + 0x0A) = 0x28A

bits	description	acc	
0-11	Read last EVENT HIGH NUMBER	R	
0-11	Write EVENT HIGH NUMBER in FIFO	W	Should be used only for ROS debugging.

SECTOR COLLECTOR DATA (ROSCTRL + 0x0C) = 0x28C

bits	description	acc	
0-15	Write SECTOR COLLECTOR data in SECTOR COLLECTOR FIFO	W	Should be used only for ROS debugging.
0-8	SECTOR COLLECTOR FIFO occupancy (16 bits words)	R	

BUNCH COUNTER FIFO OCCUPANCY (ROSCTRL + 0x0E) = 0x28E

Reset by a hard reset.

bits	description	acc
0-7	BUNCH COUNTER FIFO maximum occupancy registered	R
15	Generate local VME trigger at ROS.	W

EVENT COUNTER FIFO OCCUPANCY (ROSCTRL + 0x10) = 0x290

Reset by a hard reset.

bits	description	acc
0-7	EVENT LOW FIFO maximum occupancy registered	R
8-15	EVENT HIGH FIFO maximum occupancy registered	R

These two registers store the maximum occupancy of the corresponding FIFOs since last global reset.

These FIFOs are 255 words deep, and store the Bunch and Event counter values received from the TIM module through the TIM backplane. Once the ROS has finished processing one event, it will look at these FIFOs to see if there is any event pending and will start processing it. Therefore, if these FIFOs are full at any time, some L1As may be lost.

L1A FIFO THRESHOLD (ROSCTRL + 0x12) = 0x292

Reset by a hard reset.
Default value 0xC8 (200 L1As)

bits	description	acc
0-7	Threshold of the L1A FIFO	R/W

In this register you can program the threshold over which the ROS will send a L1A FIFO Warning Overflow error .

ORBIT LOW COUNTER (ROSCTRL + 0x14) = 0x294

Reset by a hard reset.

bits	description	acc
0-15	Orbit counter (bits 0-15)	R

ORBIT HIGH COUNTER (ROSCTRL + 0x16) = 0x296

Reset by a hard reset.

bits	description	acc
0-7	Orbit counter (bits 16-23)	R

These registers are internal counters in the ROS that is incremented at each Bunch reset signal, i.e., it will count the number of orbits. This value can be sent within the data flow in the Bunch reset counter debugging word.

Cambio el orbit counter y lo pongo sólo de 16 bits, no me cabe.

EVENT ID COUNTER (ROSCTRL + 0x18) = 0x298

Default value = 0xFFF
Reset by a soft reset and by an event reset signal from the TTC.

bits	description	acc
0-11	Event ID counter	R/W

This register is an internal counter in the ROS that is incremented when a L1A is received from any of the sources only if they have been enabled, that is:

- Local L1A generated from a VME access (bit 15 of register ROSCTRL+0x02).
- AutoL1A from the SECTOR COLLECTOR (Only if it has been enabled by writing a 1 on bit 7 of register ROSCTRL+0x02).
- L1A from the TTC system. (Only if it has been enabled by writing a 0 on bit 8 of register ROSCTRL+0x02).

This is the event ID that will be sent in the ROS Event Header word if ROS internal Event counter is selected (bit 9 of register ROSCTRL+0x02). Note that as the Event ID received from the TTC system, the first L1A will be marked with Event ID = 0, so in principle its value will be one less than the number of L1As received.

Also, note that if internal event ID is selected, the L1As will not be stored in a FIFO, therefore, if a L1A is received while the ROS is still processing a previous event, the event ID counter will be incremented, and when the ROS finishes, it will start to process the next event with the event ID value that it reads from the counter, so an event ID misalignment will happen.

TTC COMMAND RECEIVED (ROSCTRL + 0x1A) = 0x29A

Default value = 0x0
Reset by a hard reset.

bits	Description	acc
0-3	Command received from the TTC.	R

Implemented commands:

- Orbit Counter reset (command = "1000" ➔ BGo = 0x20)
- TTC Hardreset (command = "0110" ➔ BG0 = 0x18)
- Start of Gap (command = "1011" ➔ BG0 = 0x2C)
- TTCreset event size (command = "1100" ➔ BG0 = 0x30)

TTC COMMANDS: RESYNC AND HARDRESET

ROS will receive the RESYNC command and it can be checked in this register, but it will not react to it (it does nothing). It reacts to the Event counter reset that follows a resync and in such a case, it performs a soft reset if it has been programmed in that way (see ROSVME registers).
The HARDRESET TTC command is also received. DO NOT MIX this hardreset with what is used in this text as hard reset, which is an internal ROS hard reset.
If the ROS has been configured in a way to react to the HARDRESET TTC command (see ROSVME registers), it will load the CEROS and ROSCTRL FPGAs on reception of the command.

MAX EVENT SIZE (ROSCTRL + 0x1C) = 0x29C

Default value = 0x0
Reset by a hard reset (not with a resync) or by the BGO command TTCreset event size (command = "1100" ➔ BG0 = 0x30)

bits	description	acc
0-15	Maximum size of a ROS event.	R/W

6 ROS-25 CONFIGURATION

6.1 Mode of operation: Memory readout.

- Ros reset (**hard reset**): Write 0x4000 in Base+0x380. Wait 1 second for the GOL to be reset.
- Check that **FPGAs have been properly programmed**. Bits 2 to 6 are = 1 in Base+0x380. If not, try to reprogram, write 0x3E0 in ROSVME+0x8
- **CHECK GOL and QPLL**: If in Base+0x392, bits 10,9,7,6,4,2 are different from 0 and bits 5, 3 are different from 1 try the procedure to power off and on the GOL:
    - POWER OFF GOL: Write 0x4 in Base+0x392, sleep 800 ms
    - POWER ON GOL: Write 0 in Base+0x392, sleep 800 ms, Write 0 in Base+0x392.
- **Write PAF value** in Base+CEROSXX + 0xC. (5 times, one per CEROS)
- **Load paf values**: Write 0x800 in Base+0x380. (Note that this register has other bits that should not be modified unless desired, check first those bits.)
    - Optional: Read PAF values and check they match: Read Base+CEROSXX+0x40-0x4A. (25 times, one per channel)
- **Mask channels** not used in Base+CEROSXX+0x0. (5 times)
- Set **Timeout value for input channels**: Write in Base+CEROSXX+0x16. (5 times)
- Set **Maxwords limit for input channels**: Write in Base+CEROSXX+0x18. (5 times)
- Set **TTS values for input channels**: Write in Base+CEROSXX+0x50. (5 times)
- Write **Timeout value for CEROS** and **option send debug word ROS status**: Write in Base+0x284.
- Write **L1A FIFO threshold** for error warning overflow word: Write in Base+0x292.
- Write **FPGA Control Options for reprogramming FPGAs with a TTC hardreset**: Write in Base+0x388.
- Optional (if ROS reading) Write Max events or words to copy into ROS memory: Write in Base+0x30A.
- Optional (if ROS reading) Reset ROS memory pointer: Write 0x4 in Base+0x304.
- Optional (if ROS reading) Enable transfer mode: Write 0xA in Base+0x300.

- **Send a SOFT RESET**: Write 0x8000 in Base+0x380. **(NOTE: Here you should also specify other settings for the ROSVME Control and Status Register**. If bit 8 wants to be set to 1, should also be set now).
- Send **CEROS disable options** (this will also erase the BLOCKED CHANNELS FLAGS): Write in Base+CEROSXX+0x2.
- **Erase Error reg1: Write 0 in Base+CEROSXX+0x52 (5 times).**
- **Erase Error reg2: Write 0 in Base+CEROSXX+0x54 (5 times).**
- **Erase Error reg3: Write 0 in Base+CEROSXX+0x56 (5 times).**
- Send **ROSCTRL disable options (Enabling the L1As and enabling SC readout, etc)**: Write in Base+0x282.

Optional: Program interruptions.

For example, program interruption by "memory done" at level 2 with an interruption vector of 0xC4:
Write 0xC444 at ROSVME + 0x06.

Procedure for the data acquisition from ROS internal memory.

Send N L1A through the TTC system.
Wait until Memory Done = 1. (bit 1 of register ROSVME+0x00)
If you want to read the memory contents before Memory Done=1 then you would have to disable the transfer from FIFOs to memory. Write a 0 in bit 1 of register ROSMEM+0x00.
Read memory pointer.
Read from the memory the number of 16 bits words specified by the memory pointer.
Reset memory pointer.
Enable again the transfer mode. Write 0xA in Base+0x300.

6.2 Check ROS status

In order to check that the readout and the ROS-25 is behaving properly, there is some checks that can be done after configuration and periodically:

- Check that all the **FPGAS have been properly programmed**.
  - (ALARM if ROS Base+0x380 bits 2 to 6 are = 0 in, unless that CEROS is masked). Bit 2 is CEROS0, 3 CEROS1, 4 is CEROS2... 6 is ROSCTRL. ROSCTRL is never masked, if that FPGA is not programmed that ROS should be masked, it is a critical error).
- Check **GOL and QPLL register** ROSVME+0x12. (WARNING if bit4!=0. ALARM if bit 2=1, bit 3=0, bit 5=0, bit 6=1,bit 7=1, bit 9=1 or bit 10=1).
- Check if any **CEROS Timed Out**. Bits 0 to 4 of ROSCTRL+0x0. (WARNING error if different from 0, except if it is masked).

- Check **Bunch Counter Fifo Max occupancy** reg. ROSCTRL+0xE and **Bunch ID fifo full** registered (bit 7 ROSCTRL+0x0).

- Check the **parity of the number of 16 bit words transmitted**, TXENA_PAR (bit 15 of ROSCTRL+0x0). (WARNING if =1)

- Check the maximum ROS event size in terms of number of 32 bit words transmitted (ROSCTRL+0x1C)

- Check that the **status of the input channels** is ok (depends on which channels are connected). Following things to check:
    - **Unlock flags.** Bits 0 to 5 of CEROSX+0x0 (Only bit 0 for CEROS4). (WARNING if bits 0-5 =0 in CEROSX+0x0, except when it is masked) In CEROS 4 only bit 0 makes sense.
    - **Have unlock flags.** Bits 6 to 11 of CEROSX+0x4 (Only bit 6 for CEROS4). (WARNING if different from 0, except when it is masked)
    - **Event id misalignment flags.** Bits 6 to 11 of CEROSX+0x8 (Only bit 6 for CEROS4). (WARNING if different from 0, except when the channel is masked)
    - **Have timeout flags**. Bits 0 to 5 of CEROSX+0x4 (Only bit 0 for CEROS4). (WARNING if different from 0, except when it is masked)
    - **PAF flags.** Bits 6 to 11 of CEROSX+0x6 (Only bit 6 for CEROS4). (WARNING if different from 0, except when it is masked)
    - **Fifo Full flags.** Bits 6 to 11 of CEROSX+0xA (Only bit 6 for CEROS4). (WARNING if different from 0, except when it is masked)
    - **Max words reached flags.** Bits 0 to 5 of CEROSX+0xA (Only bit 0 for CEROS4). (WARNING if different from 0, except when it is masked)

- Additionally, you can check further information regarding **status of input channels**:
    - **Fifo Disparity counter.** One per CEROS (5). Bits 15 to 0 of CEROSX+0x14. (WARNING if different from 0)
    - **Fifo PAF counters** 0-5 (CEROSX+0x20-0x2A). One per input channel (25).

- If you are **working with Resynch commands** (event resets) that will generate a soft reset and erase the error values, you may check also the permanent error registers to keep track if anything has happened through all the run.
    - **Channels blocked resynch indep. (It is a summary of the following).** Bits 10 to 15 of CEROSX+0x2 (Only bit 10 for CEROS4). (WARNING if different from 0, except if it is masked)
    - **Channels have unlock resynch indep.** Bits 0 to 5 of CEROSX+0x52 (Only bit 0 for CEROS4). (WARNING if different from 0, except when it is masked)
    - **Channels event ID mis resynch indep.** Bits 0 to 5 of CEROSX+0x54 (Only bit 0 for CEROS4). (WARNING if different from 0, except when it is masked)
    - **Channels Fifo full resynch indep.** Bits 6 to 11 of CEROSX+0x54 (Only bit 6 for CEROS4). (WARNING if different from 0, except when it is masked)
    - **Channels max words resynch indep.** Bits 0 to 5 of CEROSX+0x56 (Only bit 0 for CEROS4). (WARNING if different from 0, except when it is masked)

- **Channels PAF resynch indep.** Bits 6 to 11 of CEROSX+0x56 (Only bit 6 for CEROS4). (WARNING if different from 0, except when it is masked)

- If you are working with the TSC (Sector Collector) channel enabled, you should also check:
  - **Sector Collector FIFO full,** bit 6 of ROSCTRL+0x0 (WARNING if =1).
  - **Sector Collector has timed out**. Bit 5 of ROSCTRL+0x0. (WARNING if =1, except when it is masked)

7 ROS-25 DATA FORMATS

When the ROS receives the data from the ROBs, it stores it in one 4 kBytes FIFO per channel, and at the reception of an L1A signal, it starts to read the data from the FIFOs and sends it to a common bus to the GOL serialiser.

In principle, ROS will be operated in normal mode, with a TIM module in the same crate and receiving the L1A signal from the TIM through the custom backplane.

In general, at the reception of a L1A, the ROS will send a ROS header (called "Event header") that will include the 24 bits of the ROS event ID. After that, the ROSCTRL module will start a read-out mechanism passing the token to each CEROS using a star topology. After each CEROS has performed the read-out of its channels, they will return the token to the ROSCTRL that will send it to the following CEROS.

It is important to know that at each CEROS, unless this feature is disabled, all the data packets that only contain headers and trailers and not time information or errors signalling will be discarded, in order to reduce the total throughput.

The data coming from the ROBs will be modified at each CEROS, in order to include other necessary information.

7.1 ROS-25 Control words

7.1.1 Event Header from ROS

Event header: event header from ROS

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ROS	0	0	0	1	1	1	1	1	TTC Event Counter																							
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This event header encloses all the data belonging to one event. In this word, it is included the event ID of the event that is being processed, either it comes from the TIM module or from the ROS internal event counter.

7.1.2 Event trailer from ROS

Event trailer: event trailer from ROS

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ROS	0	0	1	1	1	1	1	1	TFF	TXP	L1A_fifo_occupancy (bits 7 downto 2)						Event Word count (words of 32 bits)															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Here there is also a word count field for all the 32 bit words of the processed event, including ROS event header and trailer. The other fields in this word are:

- **TFF**: When it is 1, it indicates that any of the L1A FIFOs (Bunch counter, Event counter high or low) has been full at any time. These FIFOs store the number of events that are pending to be processed.

- **TXP**: transmitter parity error. This bit is set to 1 if the number of 16 bits words transmitted to the GOL is odd, i.e., the ROS is not working fine.

- **ECHO**: These two bits are the two higher bits (7 and 6) of the value of the occupancy of the Event Counter High FIFO, which stores the higher 11 bits of the event ID only in the case it has been received from the TIM.

- **ECLO**: It is the same that the ECHO bits but for the FIFO that stores the lower 11 bits of the event counter.

- **BCO**: It is the same that the ECHO bits but for the FIFO that stores the bunch counter.

It is important to take into account that when the L1A is not received from the TIM module, the TFF, ECHO, ECLO and BCO fields have no sense. This also implies, as said before, that the L1A rate should be slow enough to allow the ROS to process each event before receiving a new one, as overlapping triggers are not allowed in this mode.

7.1.3 Error flags from ROS

Errors: error flags sent when error condition is detected

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ROS	1	1	0	1	1	1	1	1	Error type			Link/ROB ID					1															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Error types:

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Link timed out			ROB ID					1	R									EVID mis	PAF	EF	LK	HU	FF
0	Sector Collector time out			25					1	R											EF			FF
1	Event number misalignment			ROB ID					1	R			Event ID at ROS											
2	Channel FIFO almost full			ROB ID					1	R									EVID mis	PAF	EF	LK	HU	FF
3	Channel FIFO full			ROB ID					1	R									EVID mis	PAF	EF	LK	HU	FF
3	Sector Collector FIFO full			25					1	R											EF			FF
4	Ceros timed out			31					1	R									Ceros ID					
5	Max number words			ROB ID					1	R									EVID mis	PAF	EF	LK	HU	FF
6	Warning Overflow L1A Fifo			31					1	R														
	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits 16 to 20 indicate the number of the channel that produced the error and bits 21 to 23 specify the type of error that is being reported, it can be any of the following:

- **Link timed out**: Each FPGA device will wait a programmable time when it tries to read an input FIFO but that channel is still empty. After that time, if the channel FIFO is still empty, an error word will be generated and the channel may be blocked.

As in other error words, all the status flags corresponding to that channel will be included in the error word:

- **PAF**: Indicates that the FIFO is over the almost full limit programmed.
- **EF**: Indicates that the FIFO is empty
- **LK**: Indicates if the channel is locked at that moment.
- **HU**: Indicates that the channel has been unlocked at any moment.
- **FF**: Indicates that the FIFO has been full at any time.
- **EvID mis**: Indicates that at some point the event ID read at this channel did not match the ROS event ID.

If the channel that has timedout or which FIFO is full is the Sector Collector (Channel ID = 25), only EF and FF flags will be included in the error word.

- **Event number misalignment:** In the case that the event ID received from the TIM does not match the event ID that is included in the TDC group headers, the ROS generates an error word. Note that the events are not re-aligned, as the misalignment may come from a wrong number in the event field while the data may really belong to this event. Only a track fitting can really determine to which event the data belongs to.

- **Fifo full:** This word is generated when any channel FIFO is full. If this happens, further words received will be lost.

- **Ceros timed out**: It may happen that a full group of 6 channels (a CEROS) is not working properly. If it keeps the token longer than a programmable time, it may be disabled and an error word will be generated. The timeout controller is reset when the CEROS starts to read a new channel, therefore, the timeout value should be larger than the expected time to process an event in one channel.

- **Max number of words**: This error word is generated when the ROS is reading one channel and reads out more than 200 words from a FIFO without finding a ROB trailer. If this happens, it is considered that either the data stored at that FIFO is not valid or that this channel has too much noise.

- **Warning Overflow L1A FIFO**: This error word is generated when the occupancy of the L1A Fifo of the ROS is over the programmed limit.

If Bit 14 (R) is set to one, it means that the DDU will go into Out-of-synch status or Warning Overflow when the number of error words is above a programmable limit. This bit in the error words can be enabled or disabled as desired by writing in CEROS register 0x50.

7.2 ROS-25 Debugging data

Debugging data

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ROS	1	1	1	1	1	1	1	1	Debug type			XXX					1															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Debug types:

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Bunch number			XXX = 31					1				TTC Bunch Counter											
1	BcntResCntLow			XXX = 31					1	Bcnt_res Counter Low														
2	BcntResCntHigh			XXX = 31					1							Bcnt_res Counter High								
3	CEROS STATUS			CEROS ID					1	0	0	0	evidmis				dontread							
4	ROS STATUS			XXX = 31													CEROS ID is timedout							
	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

It can be programmed if I want to send the CEROS STATUS word or not, but the ROS STATUS word will always be sent whenever a CEROS is blocked (has timedout), it is not possible to mask this word (shouldn´t introduce too much overload).

This information is to be used for debugging the ROS or the full system; in principle, is not necessary to use it in normal mode. These words can be differentiated from the TDC debugging data because bit 15 is set to 1. Bits 23 to 21 indicate the type of debug word that is going to be sent, the possibilities are:

- **Bunch number**: Bits 11 to 0 will include the Bunch ID received from the TIM through the backplane.
- **Bcnt_ResCnt High and Low**: The Bcnt_res Counter Low field contains bits 14 to 0 of the number of bunch counter resets (orbits) that have been received. Bcnt_res Counter High contains bits 23 to 15.

7.3 Generated at HPTDC, modified by ROS-25.

Group header: event header from master TDC (one per ROB)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDC	0	0	0	0	TDC ID				Event ID												Bunch ID											
ROS	0	0	0	ROB ID (0-24)					Event ID												Bunch ID											
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Group trailer: event trailer from master TDC (one per ROB)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDC	0	0	0	1	TDC ID				Event ID												Word count (32 bits words)											
ROS	0	0	1	ROB ID (0-24)					Event ID												Word count (32 bits words)											
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

TDC header: event header from TDC (master and slaves)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDC	0	0	1	0	TDC ID				Event ID												Bunch ID											
ROS	0	1	0	0	PC	PAF	TDC ID		Event ID												Bunch ID											
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

TDC trailer: event trailer from TDC (master and slaves)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDC	0	0	1	1	TDC ID				Event ID												Word count (32 bits words)											
ROS	0	1	1	0	PC	PAF	TDC ID		Event ID												Word count (32 bits words)											
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Leading measurement: single edge (normal time measurement)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDC	0	1	0	0	TDC ID				Channel					Leading time																		
ROS	1	0	0	0	PC	PAF	TDC ID		Channel					Leading time																		
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Leading measurement: combined measurement of leading and trailing edge

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDC	0	1	0	0	TDC ID				Channel					Width							Leading time											
ROS	1	0	0	0	PC	PAF	TDC ID		Channel					Width							Leading time											
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Trailing measurement

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDC	0	1	0	1	TDC ID				Channel					Trailing time																		
ROS	1	0	1	0	PC	PAF	TDC ID		Channel					Trailing time																		
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Errors: error flags sent when error condition is detected

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDC	0	1	1	0	TDC ID													Error flag														
ROS	1	1	0	0	PC	PAF	TDC ID											Error flag														
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Debugging data: separator

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDC	0	1	1	1	TDC ID				0	0	0	0									Bunch ID											
ROS	1	1	1	0	PC	PAF	TDC ID		0	0	0	0									Bunch ID											
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Debugging data: L1 buffer occupancy

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDC	0	1	1	1	TDC ID				0	0	0	1											GR		L1 occupancy						
ROS	1	1	1	0	PC	PAF	TDC ID		0	0	0	1											GR		L1 occupancy						
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Debugging data: trigger and readout FIFO occupancy

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDC	0	1	1	1	TDC ID															Trigger fifo				F	Read-out fifo							
ROS	1	1	1	0	PC	PAF	TDC ID													Trigger fifo				F	Read-out fifo							
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

As can be seen, the identification of the TDC Master that was in the HPTDC data has been replaced by the information of the number of link (ROB) that the data belongs to (links from 0 to 24). Moreover, the Sector Collector data is treated as if it was another link, link number 25.

The remaining fields have been left basically as they came from the HPTDC, so we will just make a few comments on the main differences:

- **PC**: (Parity check). The parity, calculated over each byte is transmitted from the ROB within the data flow, and it is stored in the input fifo at the ROS. The FPGA device checks if the parity is correct over the four bytes of each 32 bits word and signals it with a 0 if it is correct. If the bit is 1, this 32 bit word should be discarded as any or more bits might have flipped.

- **PAF**: (Programmable Almost Full). If this bit is set to 1, the FIFO at that particular channel has less empty words than the programmed value. By using this flag, the DAQ system can be informed that a FIFO is almost full.

7.4 Sector Collector Trigger Data

7.4.1 Sector Collector header.

Sector Collector header

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ROS	0	0	0	25					ROS Event ID															SC fifo occupancy (16 bits words)								
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

The SC header includes the least significant 11 bits of the ROS event ID. It also includes information of the occupancy of the SC fifo located at the ROS, where the data received from the contiguous SC board is stored.

7.4.2 Sector Collector trailer

Sector Collector trailer

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ROS	0	0	1	25													Word count (words of 32 bits)															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

The SC trailer includes a 16 bit word count of the number of SC 16 bits words that have been transmitted. The expected number of 16 bit words to be transmitted per event is ~ 80.

7.4.3 Sector Collector data

Sector Collector Data

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ROS	1	0	0	25													SC Data															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Finally, the SC data is transmitted in the 16 least significant bits of the SC data packet.

8 INTERFACE TO THE VOLTAGE, CURRENT AND TEMPERATURE SENSORS.

At the ROS there are three sensors that allow measuring each of the three voltages used at this board (5 V, 3.3 V and 1.8 V), measure their corresponding currents and performing temperature monitorization.

These sensors (DS2438) are 1-wire devices, which can be accessed through an I2C to 1-wire interface (DS2482). Channel 0 of the DS2482 is connected to DS2450 device for reading the laser transmitter optical power (this is not explained in this version of the manual). The other three channels are connected as indicated in the table:

Channel number	Sensor	VAD	VDD	Current
Channel 1	5 V sensor	5 V	3.3 V	5 V
Channel 2	3.3 V sensor	3.3 V	3.3 V	3.3 V
Channel 3	1.8 V sensor	1.8 V	3.3 V	1.8 V

The VME to I2C interface is implemented through the device PCA9564 [3]. There is only one PCA9564 device to perform I2C access, both to the GOL and to the DS2482 bridge to the sensors. To choose among both I2C buses, a bit has to be enabled on register " I2C & 1-wire & GOL & QPLL (ROSVME+0x12)":

- Write a 1 in bit 0 for enabling access to the GOL.
- Write a 1 in bit 1 for enabling access to the 1-wire sensor.

Setting both bits to 1 is not allowed, having priority the I,V,T 1-wire sensor.

In the following picture, a diagram of how the different devices are interconnected at the ROS is presented:

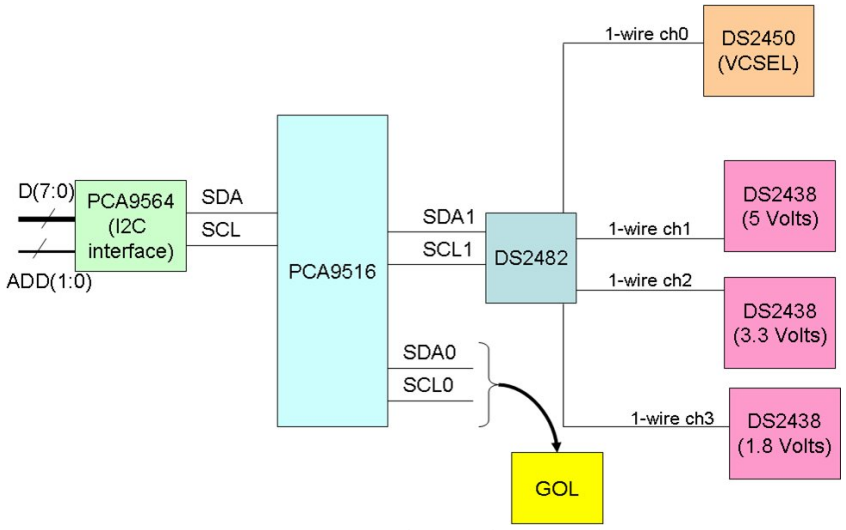

Figure 7: Diagram of the I2C buses at the ROS.

8.1 I2C interface through the PCA9564

As can be seen in its datasheet [3], the PCA9564 device has 4 registers (Status, Data, Own address and Control), which can be accessed directly as ROS registers. Here we present again the corresponding registers at the ROS for the PCA9564 used for reading the sensors and for the PCA9564 used for interface with the GOL. (Remember that ROSVME=ROS Base Address + 0x380).

PCA_STATUS (ROSVME + 0x20)

bits	description	acc	default
0-7	Status	R	0xF8
0-7	Time-out	W	0xFF

PCA_DATA (ROSVME + 0x22)

Default = 0x00

bits	description	acc
0-7	Data	R/W

PCA_ADDRESS (ROSVME + 0x24)

Default = 0x00

bits	description	acc
0-7	Own address	R/W

PCA_CONTROL (ROSVME + 0x26)

Default = 0x00

bits	description	acc	description
7	AA	R/W	Assert acknowledge flag
6	ENSIO	R/W	SIO enable bit
5	STA	R/W	Start flag
4	STO	R/W	Stop flag
3	SI	R/W	Serial interrupt flag
2-0	CR	R/W	Serial clock rate

CR: Serial clock frequency

000	330 kHz
001	288 kHz
010	217 kHz
011	146 kHz
100	88 kHz
101	59 kHz

110	44 kHz
111	36 kHz

The procedure for writing and reading via I2C is described in the PCA9564 datasheet; however, we include here a summary of routines Write_PCA(out p_add, out p_data) and Read_PCA (out p_add, in p_data), where p_add is the I2C address of the device you want to communicate with and p_data is the 7 bit data to send or receive.

The PCA9564 will be used in Master mode in every access; therefore, PCA_ADDRESS register is not needed.

The first step that has to be done is to enable SIO logic in the device at register PCA_CONTROL which requires to wait 10 ms before starting any other access. Unless this bit is disabled by the user at some point, this step needs to be done only once at the beginning. At this point, the I2C bit rate can also be selected on this register.

The next steps are summarized in what follows:

I2C WRITE ACCESS THROUGH THE PCA9564

Write_PCA(out p_add, out p_data)

1) Check PCA9564 status register, it has to be 0xF8. (Read ROS_Base_Add + 0x3A0).
2) Send START (Write 0x60 in ROS_Base_Add + 0x3A6).
3) Wait until interrupt flag (SI) is asserted. (Read bit 3 of ROS_Base_Add + 0x3A6).
4) Check status, it has to be 0x08. (Read ROS_Base_Add + 0x3A0).
5) Send the I2C address of the device you want to access to by writing p_add in bits 7 to 1 and a 0 (write) in bit 0 of PCA_DATA. (Write p_add & '0' in ROS_Base_Add + 0x3A2).
6) Reset SI flag. (Write 0x40 in ROS_Base_Add + 0x 3A6).
7) Wait until interrupt flag (SI) is asserted. (Read bit 3 of ROS_Base_Add + 0x3A6).
8) Check status, it has to be 0x18. (Read ROS_Base_Add + 0x3A0).
9) Send the data byte that you want to write by writing it in PCA_DATA. (Write p_data on ROS_Base_Add + 0x3A2).
10) Reset SI flag. (Write 0x40 in ROS_Base_Add + 0x 3A6).
11) Wait until interrupt flag (SI) is asserted. (Read bit 3 of ROS_Base_Add + 0x3A6).
12) Check status, it has to be 0x28. (Read ROS_Base_Add + 0x3A0).
13) Send a STOP condition. (Write 0x50 to ROS_Base_Add + 0x3A6).
14) Check status, it has to be 0xF8. (Read ROS_Base_Add + 0x3A0).

I2C READ ACCESS THROUGH THE PCA9564

Read_PCA (out p_add, in p_data)

1) Check PCA9564 status register, it has to be 0xF8. (Read ROS_Base_Add + 0x3A0).
2) Send START (Write 0x60 in ROS_Base_Add + 0x3A6).
3) Wait until interrupt flag (SI) is asserted. (Read bit 3 of ROS_Base_Add + 0x3A6).

4) Check status, it has to be 0x08. (Read ROS_Base_Add + 0x3A0).
5) Send the I2C address of the device you want to access to by writing p_add in bits 7 to 1 and a 1 (read) in bit 0 of PCA_DATA. (Write p_add & '0' in ROS_Base_Add + 0x3A2).
6) Reset SI flag. (Write 0x40 in ROS_Base_Add + 0x 3A6).
7) Wait until interrupt flag (SI) is asserted. (Read bit 3 of ROS_Base_Add + 0x3A6).
8) Check status, it has to be 0x40. (Read ROS_Base_Add + 0x3A0).
9) Reset SI flag. (Write 0x40 in ROS_Base_Add + 0x 3A6).
10) Wait until interrupt flag (SI) is asserted. (Read bit 3 of ROS_Base_Add + 0x3A6).
11) Read the data received from the device from PCA_DATA. (Read p_data from ROS_Base_Add + 0x3A2).
12) Check status, it has to be 0x58. (Read ROS_Base_Add + 0x3A0).
13) Send a STOP condition. (Write 0x50 to ROS_Base_Add + 0x3A6).
14) Check status, it has to be 0xF8. (Read ROS_Base_Add + 0x3A0).

8.2 1-Wire Interface to the DS2438 through the DS2482.

8.2.1 Brief introduction to DS2482.

As we said before, in order to retrieve the information from the DS2438 sensor we will use the DS2482 I2C to 1-Wire (1-W) bridge.

As an I2C slave of the PCA9564, the DS2482 has a slave address set by three pins (AD0, AD1, AD2) that, in our case, are connected to ground. Therefore, its address value (*slave-add*) is 0x18 (see datasheet [7]).

From all the DS2482 functionality, only some commands will be necessary:

- "Channel Select" (command code 0xC3), used to select one among the 8 output channels.
- "Set Read Pointer" (command code 0xE1), needed for selecting one of the different internal registers that this chip has. The command must be followed by the code of the specific register which will be used in further commands. (see datasheet for codes of different registers). The execution of other commands may set the read pointer to a different value; therefore, it will be necessary to reassign its value, using this command, before executing another one.
- "1-Wire Reset" (command code 0xB4), used to start the transaction cycle specified by 1-W protocol. In fact, this command should be sent first, before all other commands sent to the DS2438.
- "1-Wire Read Byte" (command code 0x96), used to read 1 byte from the 1-W channel. Before doing this, previous commands should instruct 1-W slave IC to prepare information that is going to be read.

- "1-Wire Write Byte" (command code 0xA5), needed for writing 1 byte to the 1-W slave. It must be followed by the byte to be written in a unique transaction.

Many operations may modify one or more bits on the internal registers of DS2482, but we only need to pay special attention to two of them: "Status Register" and "Read data register".

The "Status Register" has the "1WS" bit (bit number 0) which indicates the status of the channel that is being used in a transaction. If this bit is HIGH, the last command executed is still being processed, so it's not possible to send nor receive data (even commands) to that channel. It's necessary to wait until this bit turns into LOW state (polling it) before executing new commands.

The "Read data register" is used to retrieve data read after a "1-Wire Read Byte" command.

8.2.2 Brief introduction to DS2438.

As DS2482, DS2438 has many commands and registers, but not all of them are needed for our purposes. Registers are organized in memory pages (9 bytes in length) instead of individually addressable bytes.

This forces to manage/retrieve complete pages before getting specific bytes, even significant bits. Doing this involves the management of an intermediate memory area, called scratchpad area (with corresponding scratchpad pages), where results must be copied from DS2438 internal registers before being read by the DS2482, or where configuration data must be written before being transferred to internal DS2438 registers.

The most important page is page number 0 that contains the status/configuration register, and six additional registers which store the current, temperature and voltage information (two bytes in length for each one) once the appropriated commands have been executed. So, in fact, we will be reading and writing this page every time. Its very recommended to see DS2438 datasheet to see the specific binary data format of current, voltage and temperature because not all register bits are in use.

Due to the importance of status/configuration register, we include some datasheet paragraphs describing those bits useful for us:

> The Status/Configuration Register is a non-volatile read/write byte which defines which features of the DS2438 are enabled and how they will function. The register is formatted as follows:
>
> X ADB NVB TB AD EE CA IAD
> MSb LSb
>
> IAD = Current A/D Control Bit. "1" = the current A/D and the ICA are enabled, and current measurements will be taken at the rate of 36.41 Hz; "0" = the current A/D and the ICA have been disabled. The default value of this bit is a "1" (current A/D and ICA are enabled).
>
> CA = Current Accumulator Configuration. "1" = CCA/DCA is enabled, and data will be stored and can be retrieved from page 7, bytes 4-7; "0" = CCA/DCA is disabled, and page 7 can be used for general EEPROM storage. The default value of this bit is a "1" (current CCA/DCA are enabled).

AD = Voltage A/D Input Select Bit. “1” = the battery input (VDD) is selected as the input for the DS2438 voltage A/D converter; “0” = the general purpose A/D input (VAD) is selected as the voltage A/D input. For either setting, a Convert V command will initialize a voltage A/D conversion. The default value of this bit is a “1” (VDD is the input to the A/D converter).

TB = Temperature Busy Flag. “1” = temperature conversion in progress; “0” = temperature conversion complete.

ADB = A/D Converter Busy Flag. “1” = A/D conversion in progress on battery voltage; “0” = conversion complete, or no measurement being made. An A/D conversion takes approximately 10 ms.

Bits TB and ADB can be either polled continuously until they are done (bit LOW) or just wait time enough to ensure that the process has finished.

The process of getting sensor information involves the whole command set available in the DS2438 so we reproduce here their command codes and their functionality. A more practical explanation of their use will be presented in certain useful routines explained in further paragraphs.

Command list:

- Write Scratchpad [4EhXXh]: This command writes to the scratchpad page XXh of the DS2438. The entire 8-byte scratchpad space may be written, but all writing begins with the byte present at address 0 of the selected scratchpad. After issuing this command, the user must send the page number of the scratchpad to be written; then the user may begin writing data to the DS2438 scratchpad. Writing may be terminated at any point by issuing a reset. Valid page numbers for writing are 00h-07h.

- Read Scratchpad [BEhXXh]: This command reads the contents of the scratchpad page XXh on the DS2438. After issuing this command, the user must send the page number of the scratchpad to be read, and then may begin reading the data, always beginning at address 0 of the selected scratchpad. The user may read up to the end of the scratchpad space (byte 07h), where reserved bits will be read as 1s. Then, it can read the data CRC, and after that, all bits read will be 1s. If not all locations are to be read, the master may issue a reset to terminate reading at any time. Valid page numbers are 00h – 07h.

- Copy Scratchpad [48hXXh]: This command copies the scratchpad page XXh into the EEPROM / SRAM memory page XXh of the DS2438. After issuing this command, the user must write a page number to set which page of memory the scratchpad is to be copied. Valid page numbers are 00h - 07h. During the copy function, the NVB bit in the Status/Configuration register will be set to a “l”. When the copy is completed, this bit will set to “0”. If the bus master issues read time slots following this command, the DS2438 will output “0” on the bus as long as it is busy copying the scratchpad to SRAM/EEPROM; it will return a “1” when the copy process is complete.

- Recall Memory [B8hXXh]: This command recalls the stored values in EEPROM / SRAM page XXh to the scratchpad page XXh. This command must precede a Read SPxx command in order to read any page of memory on the DS2438. Valid page numbers are 00h – 07h.

- Convert T [44h]: This command begins a temperature conversion. No further data is required. The temperature conversion will be performed, setting the TB flag in the Status/Configuration register to a “1” during conversion. When the temperature conversion is done, the TB flag will be set to “0”. If the bus master issues read time slots following this

command, the DS2438 will output “0” on the bus as long as it is busy making a temperature conversion; it will return a “1” when the temperature conversion is complete.

- Convert V [B4h]: This command instructs the DS2438 to initiate a voltage analog-to-digital conversion cycle. This sets the ADB flag (see Status/Configuration register discussion in the Memory Map section). The voltage supply that is measured is defined by the AD bit of the Status/Configuration register. When the A/D conversion is done, the ADB flag is cleared and the current voltage value is placed in the VOLTAGE REGISTER of page 00h. While an A/D conversion is taking place, all other memory functions are still available for use. If the bus master issues read time slots following this command, the DS2438 will output “0” on the bus as long as it is busy making a voltage measurement; it will return a “1” when the conversion is complete.

Besides, DS2438 supports four access methods: *READ-ROM*, *SEARCH-ROM*, *MATCH ROM*, and *SKIP-ROM*. The first three of them are only useful in case that a 1-W channel has 2 or more slaves connected (see [8]). At the ROS board this is not necessary as each DS2438 device has an independent connection to each of the channels of the DS2482 device (only one slave).

All accesses to the DS2438 consist of transactions beginning with a *RESET-PULSE* sent by the DS2482 master, followed by a DS2438 *SKIP-ROM* command, and a sequence of simple DS2438 commands or command+parameter. After sending each byte (command or parameter), a certain time has to be waited until the serial transmission in the 1-Wire has finished. In order to know when the 1-Wire is ready to send more data, polling can be performed to bit 0 of the DS2482 status register. When this bit is 0, the 1-W bus is ready for a new access.

8.2.3 Useful basic routines

In case they are useful for the user, in what follows we have included some routines for basic actions to be performed:

struct error_code DS2482_Wait_1W_stop (timeout):

1. Read system time
2. Read DS2482 status register: ***Read_PCA (slave-add, status-value)***
3. Verify if bit-0 (1-WS) of status-value is low. If true, exit.
4. If not, verify if actual system time minus former system time, exceeds timeout parameter. If true, exit with error.
5. If not, wait (for example) 1 ms, and return to step 2.

Another useful routine is responsible for *RESET-PULSE* and *SKIP-ROM* sequence:

void RP_SkROM ( ):

1. Command the DS2482 to send a Reset Pulse: ***Write_PCA (slave-add, 0xB4).***

2. Wait until command ends: ***DS2482_Wait_1W_stop ( )***

3. Send DS2438 *SKIP-ROM* command (0xCC code). To do this it's necessary to send to the DS2482 a *1-Wire-WRITE-BYTE* command (0xA5 plus byte-to-write):
   Write_PCA (slave-add, [0xA5, 0xCC])

4. Again, wait until command ends: ***DS2482_Wait_1W_stop ( )***

Since DS2438 internal registers are organized in memory pages (9 bytes in length), it is suitable to have a procedure to read a page in one step. The procedure steps are: first, transfer information from DS2438 memory space to its scratchpad area, and then, get data bytes from the scratchpad area. This is presented in the following routine:

array_integer DS2438_read_mem_page (page_number)

1. As in other transactions, we begin with a *RESET-PULSE* and *SKIP-ROM* sequence:
   - ***RP_SkROM ( )***

2. Transfer memory-space data page to temporary (scratchpad) area. Achieving this requires to send the appropriate DS2438 command (0xB8) to the 1-W channel, and the page number of interest:
   - ***RP_SkROM ( )***
   - ***Write_PCA (slave-add, 0xB8)***
   - ***DS2482_Wait_1W_stop ( )***
   - ***Write_PCA (slave-add, page-number)***
   - ***DS2482_Wait_1W_stop ( )***

3. Next step is to point at the data bytes (scratchpad page) we want to get (code 0xBE followed by page number).
   - ***RP_SkROM ( )***
   - ***Write_PCA (slave-add, 0xBE)***
   - ***DS2482_Wait_1W_stop ( )***
   - ***Write_PCA (slave-add, page-number)***
   - ***DS2482_Wait_1W_stop ( )***

4. Finally, we should read the corresponding 9 data bytes. This action should be done right after previous step, so it is mandatory not repeating *RESET-PULSE* sequence. It involves

telling DS2482 to read a data byte from a 1-W channel (this reading automatically increments internal DS2438 memory pointer) and then get that information from DS2482 data register:

- Send DS2482 read-one-byte command: ***Write_PCA (slave-add, 0x96)***
- ***DS2482_Wait_1W_stop ( )***
- Point to DS2482 data register: ***Write_PCA (slave-add, [0xE1, 0xE1])***
- Read DS2482 data register: ***Read_PCA (slave-add, data-byte).***
- Repeat previous four steps up to nine times.

8.2.4 Detailed procedure to obtain sensor information.

Now, we proceed to explain how to read sensor's information, assuming that previous routines have already been developed.

1. First step is to select the DS2438 device to be read. To select the channel at DS2482, we have to send to the DS2482 command 0xC3 plus channel number (0xE1 for 5V sensor, 0xD2 for 3.3V sensor and 0xC3 for 1.8V sensor). Once selected, if we don't change channel number or don't reset DS2482, it remains selected, so latter communications will be done to that channel:

   Write_PCA (slave-add, [0xC3,0xE1]) ← for 5V sensor.

2. Next, it's necessary to read the status/configuration register to modify some of its bits to select or not current conversion at the DS2438 and to select the input pin where we want to read the voltage from. This register is located in byte number 0 from memory page 0:

   DS2438_read_mem_page(0)

3. Set IAD bit (bit-0 DS2438 configuration register) high to perform current conversion. Set VAD bit (bit-3 DS2438 configuration register) high for voltage measurement from VDD pin or low for voltage measurement from DS2438 chip's VAD pin.

4. Send command for writing data in page number 0. This is done by sending 3 bytes:

   - DS2438 command for writing page,
   - page number,
   - data byte to be written.

   Remember that writing a byte to the 1-Wire bus is equivalent to send DS2482 *1-Wire-WRITE-BYTE* command (0xA5 plus byte-to-write).

Actually, the operation performed by this transaction is writing data to a so-called “scratchpad page”, a kind of temporary data buffer into DS2438. After that, it's required to transfer that page into the memory space.

So, the overall procedure will be:

(Write to scratchpad page)

- *RP_SkROM ( )*
- *Write_PCA (slave-add, [0xA5,0x4E])*
- *DS2482_Wait_1W_stop ( )*
- *Write_PCA (slave-add, [0xA5,0x00])*
- *DS2482_Wait_1W_stop ( )*
- *Write_PCA (slave-add, [0xA5, value-of-control-register-modified])*

(Transfer page into memory)

- *RP_SkROM ( )*
- *Write_PCA (slave-add, [0xA5,0x48])*
- *DS2482_Wait_1W_stop ( )*
- *Write_PCA (slave-add, [0xA5,0x00])*

5. Next step is to command DS2438 to perform temperature (code 0x44) and voltage/current (code 0xB4) measurements.

   (Convert temperature)

   - *RP_SkROM ( )*
   - *Write_PCA (slave-add, [0xA5,0x44])*

   (Convert voltage/current)

   - *RP_SkROM ( )*
   - *Write_PCA (slave-add, [0xA5,0xB4])*

6. Now it is necessary to wait enough time so voltage and temperature conversion are done. It is possible to poll ADB and TB status bits so, when they are both low, we ensure that conversion has finished, but it is more simple time waiting and save accesses to the device.

7. Then, we retrieve DS2438 memory page number 0 to get bytes 1 (LSB) and 2 (MSB) with temperature information, bytes 3 (LSB) and 4 (MSB) with voltage information, and 5 (LSB) and 6 (MSB) with current information. Remainder bytes are discarded:

   DS2438_read_mem_page(0)

8. Finally, we will convert binary bytes into proper units.

$$T = (-1)^{bit15\_of\_byte\_2}\left(\frac{byte\_1}{256} + byte\_2\right)^{o}C$$

$$V = \frac{(256 \times byte\_4 + byte\_3)}{100} volts$$

$$I = \frac{1.606 \cdot 10^{-4}}{R_{sens}} \cdot (-1)^{bit15\_of\_byte\_6}(256 \times (byte\_6) + byte\_5)A$$

At ROS prototypes $R_{sens} = 0.033\ \Omega$

9 INTERFACE TO THE GOL.

The GOL (Gigabit Optical Transmitter) is an ASIC developed at CERN Microelectronics group [4] that serialises the 16 bit word data and drives an optical laser (VCSEL HFE4190-541) for transmission through optical fibber to the next step in the read-out chain, the DDU boards.

To avoid over-currents on the VCSEL transmitter at start-up, the GOL and the VCSEL are powered off by default. Therefore, when the link is going to be used, they should be turned on by writing a 0 in bit 2 of register "I2C & 1-wire & GOL & QPLL (ROSVME+0x12)".

In that register there is also a flag that indicates the status of the GOL (GOL ready (bit 3) and GOL not ready registered (bit7)). If at any time the GOL has not been ready, the GOL not ready registered flag will keep a 1, although the GOL has recovered from its error and GOL is again ready (bit 3 set to 1). This registered flag should be erased after turning on the GOL in order to reflect further problems.

It is recommended to wait around 800 ms between turning on the GOL and erasing the GOL not ready registered flag, to insure that the GOL is in the ready state. Note that the turning on of the GOL includes the power up time of the 2.5V regulator, the QPLL initialization time and the GOL initialization time.

Besides, the GOL internal registers can be accessed for configuration and monitoring through an I2C interface. This interface has been explained in previous section and the routines Write_PCA and Read_PCA can be used as detailed before.

Note: At the moment an error in the status words read from the PCA9564 has been found if the Read_PCA and Write_PCA procedure is followed. It is due to strange behaviour of the GOL I2C interface that is under study at the moment. However, the procedure as it is described works fine and access to the GOL registers can be done properly, the only difference is that status words received from the PCA9564 are not the ones indicated.

For what concerns to the I2C address of the GOL, it occupies two consecutive positions in the 7-bit wide I2C address space.

I2C access register name	I2C address
I2C_pointer	0
I2C_data	1

Data written in the first address (0) is a pointer to the corresponding GOL internal register. Therefore, at that address it should be written any of the 6 possible values of the GOL internal registers:

GOL internal registers address (I2C_pointer content)	Internal Register	Default content
0	Config 0	0x33
1	Config 1	0x1F
2	Config 2	0x10
3	Config 3	0x20
4	Status 0	0x00
5	Status 1	--

Depending on which value has been written to the I2C_pointer register, the corresponding content of the GOL internal register can be written or read from the I2C_data register.

The main parameter that may be desired to modify at the GOL is the VCSEL bias current, which can be done in register Config 3:

GOL Internal Register Config 3

Bits	Name	Description
<6:0>	LD_current/driver_strength	Defines the bias current for the Laser driver.
<7>	use_conf_regs	When 1, the content of the Configuration register 2 and 3 are used to define the value for the PLL_current and LD_current. If 0, the values are derived from the encoded values on the pads (0x00 for LD_current)

The number in bits Config3<6:0> translates the laser-diode bias current according to:

$$I = 1\ mA + Config3<6:0> \times 0.4\ mA$$

By default, the bias current is 1 mA, and the maximum bias current should be kept below 12mA, **therefore a value over 0x1B should not be programmed at Config3<6:0>**.

Also, could be interesting to read the value of the status registers:

GOL Internal Register Status 0

Bits	Name	Description
<7:0>	loss_of_lock_count	Number of “loss-of-lock”events since last reset.

GOL Internal Register Status 1

Bits	Name	Description
<7:6>	link_control_state_A	Current state of link initialisation logic A.
<5:4>	link_control_state_B	Current state of link initialisation logic B.
<3:2>	link_control_state_C	Current state of link

		initialisation logic C.
<1:0>		Set by hardware to “01”

For SEU robutness, the link initialisation logic is triplicated. The possible status are:

00: Out of lock state
01: Locked state
10 REady state
11 TX_lolc state.

For more information refer to the GOL user manual [4]

9.1 Procedure for accessing the GOL.

According to what explained before, the procedure to read or write from the GOL internal registers can be summarized as follows:

WRITE TO A GOL INTERNAL REGISTER:

1. Enable GOL I2C access at the ROS (write a 1 on bit 0 of ROS_Base_Add + 0x392).
2. Write GOL internal register address to the GOL I2C_pointer:
   Write_PCA (p_add = 0, p_data = GOL internal register address)
3. Write GOL internal register data to the GOL I2C_data:
   Write_PCA (p_add = 1, p_data = GOL internal register data)

READ FROM A GOL INTERNAL REGISTER:

1. Enable GOL I2C access at the ROS (write a 1 on bit 0 of ROS_Base_Add + 0x392).
2. Write GOL internal register address to the GOL I2C_pointer:
   Write_PCA (p_add = 0, p_data = GOL internal register address)
3. Read GOL internal register data from the GOL I2C_data:
   Read_PCA (p_add = 1, p_data = GOL internal register data)

10 APENDIX A: DATA GENERATED AT THE HPTDC (ROB).

As described before, each ROB has 4 HPTDCs in a token ring, where one of them has been configured as Master. This HPTDC will control the token of the read-out ring and is the one in charge of generating a group header and trailer that will enclose the time information generated by all HPTDCs in the ROB.

This header and trailer will contain information that allows identifying the event number and the bunch crossing the data belongs to. This information comes from internal counters in the HPTDC that are reset by signals from the TTC system, and not directly from TTC devices. These counters are 11 bits long, so their possible values are between 0 and 4095.

Typically, the HPTDCs are configured to provide the time information of the leading edge of the signals within a programmable window. This information corresponds to the leading measurement word [page 22 ref 4] and contains information of the TDC number in the ROB (from 0 to 3) and the channel that received the signal (from 0 to 31). It is important to take into account that the two least significant bits of the leading time field are not used in low resolution mode, so the value should be divided by 4 in order to obtain correct timing information. Therefore, calculating the time value of the measurement can be easily made by applying:

$$\frac{(Leading\_time)}{4} * \frac{25}{32}\, ns$$

When any HPTDC detects an error condition, i.e. buffer overflow, it signals it to the CCB board and also, it is programmed to send an error word within the data flow. The possible error flags are described in page 23 of reference [4].

Although it is not probable to use it in normal operation mode, the HPTDCs can be programmed to provide other information words such as:

- trailing measurement, where it is digitalized the time information of the falling edge of the signal,
- combined measurement of leading and trailing edge, where the obtained information is the leading time and the width of the input pulse,
- Local TDC headers and trailers, where all the HPTDCs will give headers and trailers besides the master header and trailer. In this mode, the throughput of the link is largely increased.
- and other debugging information that show the occupancies of the different FIFOs in the HPTDC.

The first four bits from each 32 bit TDC word identify the type of word generated: header, leading measurement, error word, etc.

A snap of the data flow from a ROB could be something like this:

```
.....
TDC Header: TDC ID=3 Event ID=18 Bunch ID=2186
        Time measurement: TDC ID=0 Channel=4 Time=158ns
        Time measurement: TDC ID=0 Channel=14 Time=152ns
        Time measurement: TDC ID=0 Channel=7 Time=235ns
        Time measurement: TDC ID=0 Channel=22 Time=267ns
        Time measurement: TDC ID=0 Channel=4 Time=523ns
        Time measurement: TDC ID=1 Channel=11 Time=85ns
        Time measurement: TDC ID=1 Channel=25 Time=411ns
        TDC Error: TDC ID=1 Error flag=Internal fatal error
        Time measurement: TDC ID=2 Channel=6 Time=147ns
        Time measurement: TDC ID=3 Channel=6 Time=54ns
        Time measurement: TDC ID=3 Channel=27 Time=81ns
        Time measurement: TDC ID=3 Channel=3 Time=347ns
        Time measurement: TDC ID=3 Channel=19 Time=389ns
TDC Trailer: TDC ID=3 Event ID=18 Wordcount=15

TDC Header: TDC ID=3 Event ID=19 Bunch ID=642
        Time measurement: TDC ID=0 Channel=4 Time=167ns
        Time measurement: TDC ID=0 Channel=14 Time=162ns
        Time measurement: TDC ID=0 Channel=9 Time=255ns
.....
```

It can be seen that after a header, the first data received belong to TDC 0, afterwards TDC 1, etc. Nevertheless, inside each TDC it is not in strict temporal order and not even follows a fixed channel number order. The reason of this due to the way the different read-out FIFOs are organised inside the HPTDC and the arbitration mechanism that is used to perform the trigger matching. For more information, refer to HPTDC manual.

In MB1 Minicrates, due to the little space available, one of the ROBs is a ROB-32, that is, it only has one HPTDC. This HPTDC is configured as master and will provide master headers and trailers, but usually will be configured with a TDC ID = 0.

11 REFERENCES

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[3] PCA9564 datasheet. http://www.semiconductors.philips.com/pip/PCA9564N.html

[4] GOL user manual. http://proj-gol.web.cern.ch/proj-gol/golManuals.htm

[5] TIM User manual. http://wwwae.ciemat.es/cms/DTE/idoc.htm#TIM

[6] TTCrx User Manual. http://ttc.web.cern.ch/TTC/TTCrx_manual3.11.pdf

[7] DS2482-800 datasheet: http://pdfserv.maxim-ic.com/en/ds/DS2482-800-DS2482S-800.pdf

[8] DS2438 datasheet: http://pdfserv.maxim-ic.com/en/ds/DS2438.pdf