Ciemat Centro de Investigaciones Energéticas, Medioambientales y Tecnológicas

ROS-8 User Manual

Version 2.1

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PRELIMINARY

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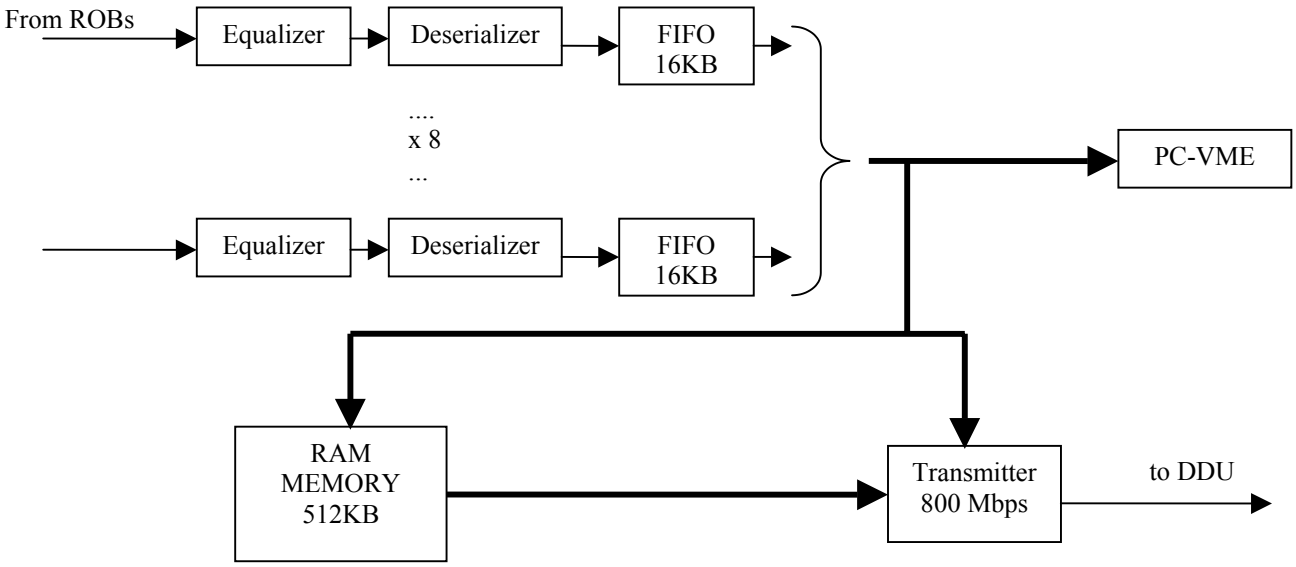
In this manual it is explained the basic functionality of the Read-Out Server (ROS) prototype with 8 input channels, developed in the CIEMAT (Madrid) for Minicrate data reading.

This is a 6U VME board with RJ-45 input and output connectors, that allows reading of up to 8 Read-Out Boards (ROBs).

In this document version, the purpose is to explain the different modes of operation of the ROS board: data read through a VME module, data stored on memories and then read through the VME module and data transferred through the Ethernet slow link.

1 ROS Description

In the following diagram it can be seen a scheme of the ROS data path.

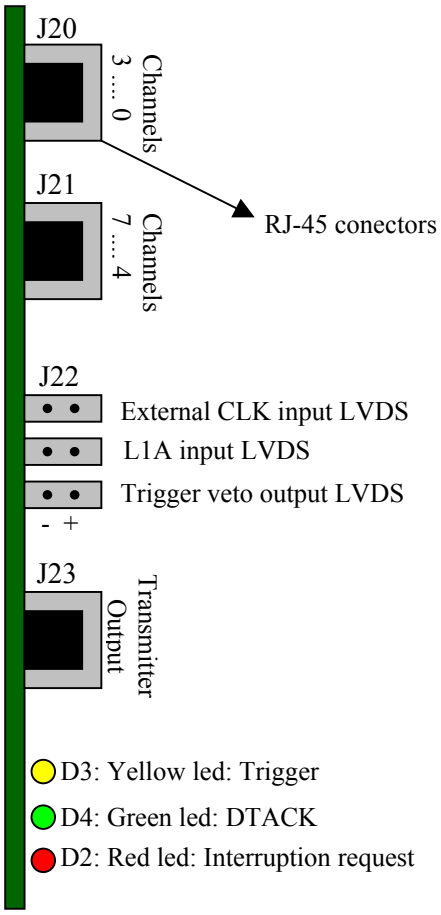


Input channels go through an equalizer that performs high-speed data recovery, and then the DS90LV1212 deserializer sends the 8 data bits plus a parity bit to the appropiate FIFO (IDT72V263) where data are stored.

There is one 16 KBytes FIFO for each channel, and they transmit their data to a common bus. Data can be read directly from the FIFOs through VME or stored in the 512Kbytes RAM memory or sent out through a Ethernet Slow (800Mbps) 8B/10B serializer.

2 ROS Connections

In the following diagram the input and output connectors of the ROS are shown:



Besides the three frontal leds that inform of the DTACK signal, Interruption request and Trigger signal, there are additional SMD leds in the board with the following purpose:

- D6: green led. Indicates the proper operation of the power supply circuitry. Whenever it is flashing it indicates a shortcircuit or any other circumstance for a high current consumption.
- D1: red led. Indicates correct programing of the U9 FPGA.
- D34, D26, D18, D14, D22, D30, D38, D10: red leds. Indicate the lock state of the deserializer. They shall turn on when the ROB is connected to the ROS and a valid code for clock recovery is being transmitted.

The jumper J16 selects between an external (J22 input) or an internal 40MHz clock:

- pin 2 connected to pin 1: internal clock
- pin 2 connected to pin 3: external clock.

There is also a switch S2 to select the U9 FPGA mode of configuration that shall be set to 0000 for configuring from the EEPROM. Push button S3 allows reprogramming of the U9 FPGA.

3 ROS Addressing

All access to this board are A24. The base address (bits A23 to A19) of the ROS can be selected with S1 switch. At least 512KB of address space shall be reserved for this board. The access may be Word accessing or Long Word accessing depending if it is to the RAM memory or to the control registers.

3.1 Access to registers: All access are Long Word.

A summary of the control registers of the ROS is shown next. It is indicated whether it is a read-only (R), write-only (W) or read and write (R/W) register.

General Control and Status Register (Base address + $00)

0-1	00 → Interrupt Disable 01 → Enable SPAE 10 → Enable SPAF 11 → Enable End of Memory	R/W	These 2 bits select and enable the source for interruptions.
2	Serializer Power Up	R/W	Enables the operation of output serializer
3	Fifo to Serializer	R/W	Enables fifo data to be transferred automatically to serializer
4	SPAE	R	Logical OR of all PAE flags
5	SPAF	R	Logical NAND of all PAF flags
6	Memory Done Memory to Serializer	R W	
7	Select Veto 0 → SPAE / 1 → SPAF	R/W	
8	Master Fifo Reset	W	Required prior to any FIFO's operation to set them in the appropriate operation mode
9	Partial Fifo Reset	W	Clears data FIFO's contents (only).
10	Load FIFO's Programmed Values	W	Loads contents of PAE and PAF Registers ($08 and $0C) into FIFO's internal registers
11	Board Reset	W	

The PAE and PAF flags are useful as a warning of whether the FIFO is near to be empty or near to be full. The number of words (offset) of margin before each flag is asserted, is programmable. A global flag for all FIFO (SPAE or SPAF) may be

programmed to perform an interruption, allowing the execution of actions as vetting triggers or any other failsafe mechanism to avoid overflow.

Receiver Control & Status Register (Base address + $04)

0-7	Receiver Power Up 1-8	R/W	Bit"x"='1' enables FIFO from channel "x".
8-15	Receiver Lock 1-8	R/W	Unlock state of serializers. A '1' is written on bit "x" whenever channel "x" has at least once be unlocked. FIFO may be full of invalid data. These bits can only be erased from VME.

Programmed Almost Empty Register (Base address + $08)

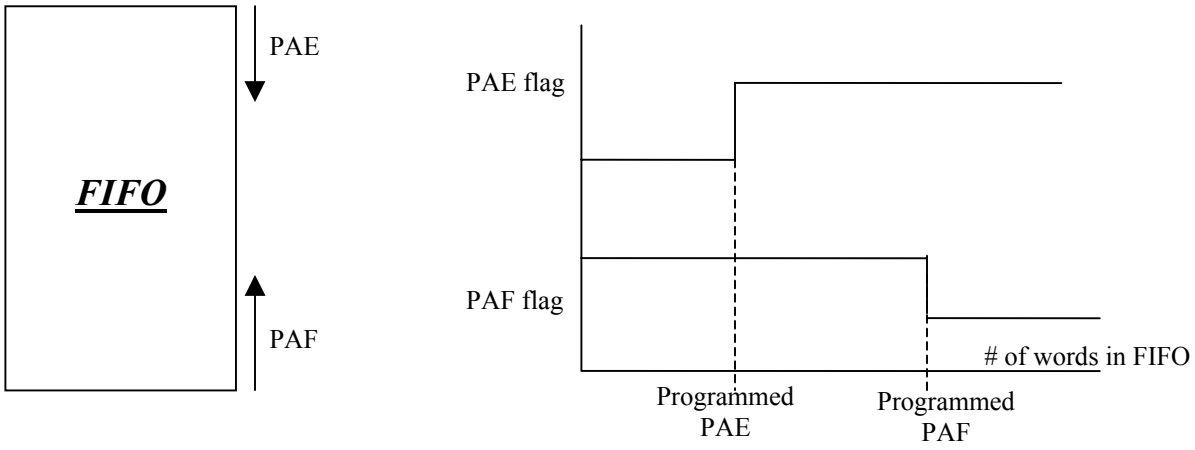
0-12	PAE	R/W	PAE value to be loaded into FIFO's registers.

The PAE value is the offset for the PAE flag, which is asserted when the number of words in the FIFO is bigger than the PAE value. PAE will be load into the FIFOs PAE registers when bit 10 from register $00 is set to '1'.

Programmed Almost Full Register (Base address + $0C)

0-12	PAF	R/W	PAF value to be loaded into FIFO's registers.

This offset represents the minimum number of empty words in the FIFO before the PAF flag is asserted. The following diagram describes PAE and PAF flags behaviour.



Fifo Full flags (Base address + $14)

0-7	FF Fifo 1-8	R	Bit "x" ='1' indicates that FIFO from channel "x" is full.
8-15	FF Latched Fifo 1-8	R	Latched values from previous flags.

PAE & PAF flags (Base address + $18)

0-7	PAE Fifo 1-8	R	PAE flags from each of the 8 FIFO´s.
8-15	PAF Fifo 1-8	R	PAF flags from each of the 8 FIFO´s.

Empty Fifo and Half Full flags (Base address + $1C)

0-7	EF Fifo 1-8	R	Empty FIFO flags from each of the 8 FIFO´s. (Active High).
8-15	HF Fifo 1-8	R	Half full FIFO flags from each of the 8 FIFO´s (Active High).

Interrupt Register (Base address + $20)

0-7	Interrupt Vector	R/W	Interrupt vector for ROS interruptions.
8-10	Interrup Level 1-7	R/W	Interrupt level for ROS interruptions.

FIFO Data Registers (Base address + $40-$5C)

0-15	Fifo 1-8 Data 0-15	R	16-bit word of data.
16	Fifo 1-8 Parity Error	R	Calculated and received does not match.
17	Fifo 1-8 Parity 0	R	Received parity of least significant byte from data.
18	Fifo 1-8 Parity 1	R	Received parity of most significant byte from data.
19	Fifo 1-8 EF	R	Empty FIFO flag at the moment of reading.
20	Fifo 1-8 FF	R	Full FIFO flag at the moment of reading.
21	Fifo 1-8 PAE	R	PAE flag of this FIFO at the moment of reading.
22	Fifo 1-8 PAF	R	PAF flag of this FIFO at the moment of reading.

Each of this registers correspond to each of the FIFOs, that is $40 to FIFO 0, $44 to FIFO 1, ...

Each access to these registers performs a new read cycle of the next FIFO word, until the FIFO is empty. Since then, the EF flag will be asserted and the data output will remain at the last read value.

PAE & PAF programmed values (Base address + $60-$7C)

0-12	PAE / PAF Values FIFO 1-8	R	Read Sequentially PAE & PAF FIFO Values

Each of this registers correspond to each of the FIFOs, that is $60 to FIFO 0, $64 to FIFO 1, ... The value read is the stored PAE and PAF value in each FIFO, sequentially one after the other. First access to these registers does not give a valid value. In order to read properly PAE and PAF values, four accesses have to be done each time.

4 VME Mode of Operation

In this mode of operation data is read through the PC with an VME access, but they are not sent to the memories nor the serializer. Notice that this will require a different mode of operation and data will probably have a different format.

4.1 ROS configuration

a) Reset the ROS (0x800 -> $00)
b) Master FIFO reset (0x100 -> $00)
c) Optional: Write PAE value (PAE -> $08) (Default offset: 511 words)
d) Optional: Write PAF value (PAF -> $0C) (Default offset: 511 words)
e) Optional: Load PAE and PAF values in the FIFOs (0x400 -> $00)
f) Enable FIFOs (For example, if you want to enable channels 7, 4, 1 y 0, you write "10010011" -> $04)
g) LOCK reset: Once enabled the channels it is necessary to erase the old latched values of lock. Write "00XX" -> $04. Where XX is the value written in step f).
h) Check the LOCK value: Read most significant byte from $04.
i) Optional: Check PAE and PAF loaded values: Read four times from register $60+4*ROS channel. First value is invalid, next value is PAE and next is PAF. Ignore last value.

4.2 Reading from ROS

a) Read sequentially from the register $40+4*ROS channel until bit 19 turns to 1. This last value when EF='1' is not valid, it is the same value that has already been read.
   Parity errors can be monitorized (bit 16) and re-checked, comparing them with bits 17 and 18. FF, EF, PAE and PAF can be monitorized also when desired.

The format of the incoming data is the same as if they were read directly from the TDC [1] but one 16-bit word at a time (most significant word first). Next it is shown an example of a normal data flow where there is one readout event with five hits.

Words	
300	TDC Master = 3 Event ID = 0 Bunch ID = 2775
AD7	
4000	TDC = 0 Channel = 0 Time (ns) = 371
76C	
4060	TDC = 0 Channel = 12 Time (ns) = 370
768	

4008	TDC = 0 Channel = 1 Time (ns) = 371
76C	
4010	TDC = 0 Channel = 2 Time (ns) = 371
76C	
4018	TDC = 0 Channel = 3 Time (ns) = 371
76C	
1300	TDC Master = 3 Event ID = 0 Wordcount = 7
7	
300	TDC Master = 3 Event ID = 1 Bunch ID = 87
1057	
....	.....

5 Memory and Serializer mode of operation

The ROS has four modules of static RAM memory of 64K words of 16 bits each, that is, 256K words of 16 bits. In order to be able to store data on memory, the trigger signal has to arrive to the ROS board through the L1A input of connector J22 (second pair). As this signal is 25 ns wide, it has to be on proper phase with the ROS clock so it can detect it, therefore an external 40MHz clock synchronous with the trigger should be also connected on J22 clock input (first pair). Jumper 16 has to be connected properly for the board to use the external clock, connecting pins 2 and 3. These indications are also necessary if we want to send the information through the copper serial Ethernet Slow link.

The steps for configuring the ROS are the same that those indicated on 4.1 plus some final steps, depending on how we want to operate.

5.1 Store data on memory

If we only want data to be stored on the memory, we need to enable bit 3 on the General Control and Status register.

After that, we start the operation and then, at any moment we can read the information from the RAM memory, accessing to the following registers in Word access mode:

FIRST WORD: Memory Access (Base address + $00)

0-15	Memory Data	R/W

SECOND WORD: Memory Access (Base address + $02)

0-15	Memory Data	R/W

.....

LAST WORD: Memory Access (Base address + $7FFFE)

0-15	Memory Data	R/W

When the memory is full it is overwritten with next incoming data.

The data that goes to the memory has a different format than the one that we can read directly from the FIFO. Detailed differences can be found in appendix A.

There is also a 18 bits memory pointer accessible from register $24 that indicates the number of 16 bits words that have been written on ROS memory.

Memory Address Pointer Register (Base address + $24)

0-17	Memory Address Pointer	R/W

5.2 Transmit through the serializer

If we want to send the data through the serializer TLK1501 we need to enable it (bit 2 of Control register) and also enable bit 3 to allow data to go directly from Fifo to the serializer. These data will be also stored on the memories. In this mode of operation the data is also in the format indicated in appendix A.

5.3 Transmit through the serializer data from memory

There is still another mode of operation in which we can store the data on the memory and then send this data through the TLK1501 link. That happens when bit 6 of the General Control register is enabled, bit 2 should also be enabled.

6 References

[1] "High Performance Time to Digital Converter". Version 2.1. J. Christiansen. CERN/EP – MIC. July 2002. Accesible from:

http://micdigital.web.cern.ch/micdigital/hptdc/hptdc_manual_ver2.1.pdf

[2] Serializer TLK1501 datasheet.
http://focus.ti.com/docs/prod/folders/print/tlk1501.html

7 Appendix A

Here it is described how the data coming from the TDC is modified to the ROS format.

Group header: event header from master TDC (one per ROB)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDC	0	0	0	0	TDC ID				Event ID												Bunch ID											
ROS	0	0	0	ROB ID (0-30)					Event ID												Bunch ID											
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Group trailer: event trailer from master TDC (one per ROB)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDC	0	0	0	1	TDC ID				Event ID												Word count											
ROS	0	0	1	Pc	TDC Master				Event ID												Word count											
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

TDC header: event header from TDC (master and slaves)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDC	0	0	1	0	TDC ID				Event ID												Bunch ID											
ROS	0	1	0	Pc	0	0	TDC ID		Event ID												Bunch ID											
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

TDC trailer: event trailer from TDC (master and slaves)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDC	0	0	1	1	TDC ID				Event ID												Word count											
ROS	0	1	1	Pc	0	0	TDC ID		Event ID												Word count											
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Leading measurement: single edge (normal time measurement)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDC	0	1	0	0	TDC ID				Channel					Leading time																		
ROS	1	0	0	Pc	0	0	TDC ID		Channel					Leading time																		
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Leading measurement: combined measurement of leading and trailing edge

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDC	0	1	0	0	TDC ID				Channel					Width							Leading time											
ROS	1	0	0	Pc	0	0	TDC ID		Channel					Width							Leading time											
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Trailing measurement

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDC	0	1	0	1	TDC ID				Channel					Trailing time																		
ROS	1	0	1	Pc	0	0	TDC ID		Channel					Trailing time																		
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Errors: error flags sent when error condition is detected

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDC	0	1	1	0	TDC ID													Error flag														
ROS	1	1	0	Pc	0	0	TDC ID											Error flag														
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Debugging data: separator

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDC	0	1	1	1	TDC ID				0	0	0	0									Bunch ID											
ROS	1	1	1	Pc	0	0	TDC ID		0	0	0	0									Bunch ID											
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Debugging data: L1 buffer occupancy

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDC	0	1	1	1	TDC ID				0	0	0	1											GR		L1 occupancy							
ROS	1	1	1	Pc	0	0	TDC ID		0	0	0	1											GR		L1 occupancy							
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Debugging data: trigger and readout fifo occupancy

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDC	0	1	1	1	TDC ID															Trigger fifo				F	Read-out fifo							
ROS	1	1	1	Pc	0	0	TDC ID													Trigger fifo				F	Read-out fifo							
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Pc: parcheck bit

Event header: event header from ROS Master

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ROS	0	0	0	1	1	1	1	1	ROS event ID								TTC L1A ID															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Event trailer: event trailer from ROS Master

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ROS	0	0	1	1	1	1	1	1	ROS event ID								Word count															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Errors: error flags sent when error condition is detected

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ROS	1	1	0	1	1	1	1	1	Error type			Link/ROB ID																				
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Error types:

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Link unlocked (IMPLEMENTED)			Link ID																				
1	Link time out			Link ID																				
2	Group Event misalignement			Link ID					expected Event ID								found Event ID							
3	Parity error (IMPLEMENTED)			Link ID																				
4	Fifo almost full			Link ID																				
5	Fifo full			Link ID																				
	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Status: status from ROS Master (once every n events)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ROS	1	1	1	1	1	1	1	1	0	0	0	Link 6			Link 5			Link 4			Link 3			Link 2			Link 1			Link 0		
ROS	1	1	1	1	1	1	1	1	0	0	1	Link 13			Link 12			Link 11			Link 10			Link 9			Link 8			Link 7		
ROS	1	1	1	1	1	1	1	1	0	1	0	Link 20			Link 19			Link 18			Link 17			Link 16			Link 15			Link 14		
ROS	1	1	1	1	1	1	1	1	0	1	1	Link 27			Link 26			Link 25			Link 24			Link 23			Link 22			Link 21		
ROS	1	1	1	1	1	1	1	1	1	0	0	Spare			Spare			Spare			Spare			Link 30			Link 29			Link 28		
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Link info:

	2	1	0
Link n	Unlocked	Time Out	Masked

8 Appendix B

ROS Registers (C4-V6)

All access A24

Memory Access (Word)

Address 0 – 524286 [0-7FFFE] (262144 words)

0-15	Memory Data	R/W

Register Access (Long Word)

Register 0 ($00)

GRP00-00 (00 00 00)
General Control & Status

0-1	00 → Interrupt Disable 01 → Enable SPAE 10 → Enable SPAF 11 → Enable End of Memory	R/W	VME_REG	etr_ctrl	enw_ctrl
2	Serializer Power Up	R/W	VME_REG	etr_ctrl	enw_ctrl
3	Fifo to Serializer	R/W	VME_REG	etr_ctrl	enw_ctrl
4	SPAE	R	VME_REG	etr_ctrl	–
5	SPAF	R	VME_REG	etr_ctrl	–
6	Memory Done Memory to Serializer	R W	VME_REG	etr_ctrl	 enw_ctrl
7	Select Veto 0 → SPAE / 1 → SPAF	R/W	VME_REG	etr_ctrl	enw_ctrl
8	Master Fifo Reset	W	VME_REG	–	enw_ctrl
9	Partial Fifo Reset	W	VME_REG	–	enw_ctrl
10	Load FIFO's Programmed Values	W	VME_REG	–	enw_ctrl
11	Board Reset	W	VME_REG	–	enw_ctrl

Register 1 ($04)

GRP00-01 (00 00 01)
Receiver Control & Status

0-7	Receiver Power Up 1-8	R/W	VME_REG	etr_rec	enw_rec
8-15	Receiver Lock 1-8	R	ROS	etr_rec	–

Register 2 ($08)

GRP00-10 (00 00 10)
Programmed PAE Value

0-12	PAE	R/W	ROS_MUX	etr_paerg	enw_paerg

Register 3 ($0C)

GRP00-11 (00 00 11)
Programmed PAF Value

0-12	PAF	R/W	ROS_MUX	etr_pafrg	enw_pafrg

Register 5 ($14)

GRP01-01 (00 01 01)
FF Status

0-7	FF Fifo 1-8	R	ROS_MUX	etr_paef / selflg=1	–
8-15	FF Latched Fifo 1-8	R	ROS_MUX	etr_paef / selflg=1	–

Register 6 ($18)

GRP01-10 (00 01 10)
PAE & PAF Status

0-7	PAE Fifo 1-8	R	ROS_MUX	etr_paef /selflg=2	–

8-15	PAF Fifo 1-8	R	ROS_MUX	etr_paef /selflg=2	–

Register 7 ($1C)

GRP01-11 (00 01 11)
EF & HF Status

0-7	EF Fifo 1-8	R	ROS	etr_efhf (/selflg=3)	–
8-15	HF Fifo 1-8	R	244	etr_efhf (/selflg=3)	–

Register 8 ($20)

GRP10-00 (00 10 00)
Interrupt

0-7	Interrupt Vector	R/W	VME_REG	etr_ivec	–
8-10	Interrup Level 1-7	R/W	VME_REG	etr_ivec	–

Register 9 ($24)

GRP10-01 (00 10 01)
Memory Address Pointer

0-17	Memory Address Pointer	R/W	MEM_CTRL	etr_mempnt	enw_mempnt

Register 13 ($34)

GRP11-01 (00 11 01)
Transmission Status 2

0-15	Last Event Number	R	ROS	etr_trst2	–

Registers 16-23 ($40-$5C)

GRP2 (010 XXX)
Data Fifo 1-8

0-15	Fifo 1-8 Data 0-15	R	ROS_MUX	etr_fifo	–
16	Fifo 1-8 Parity Error	R	ROS_MUX	etr_fifo	–
17-18	Fifo 1-8 Parity 0-1	R	ROS_MUX	etr_fifo	–
19	Fifo 1-8 EF	R	ROS	etr_fifo	–
20	Fifo 1-8 FF	R	ROS_MUX	etr_fifo	–
21	Fifo 1-8 PAE	R	ROS_MUX	etr_fifo	–
22	Fifo 1-8 PAF	R	ROS_MUX	etr_fifo	–

Registers 24-31 ($60-$7C)

GRP3 (011 XXX)
Read Sequentially PAE & PAF FIFO Values

0-12	PAE / PAF Values FIFO 1-8	R	ROS_MUX	etr_paef	–

Register 12 ($30)

GRP11-00 (00 11 00)
Register Pointer

0-7	Register Pointer	R/W	ROS	etr_trst1	enw_trst1

Registers 32-39 ($80-$9C)

GRP4 (100 XXX)
Additional Registers

Transmission Status 1 & Control ($80)

RPointer=0	0-7	Channel Time Out 1-8	R/W	ROS	etr_bcount	enw_bcount
	8-15	Mask Channel 1-8	R/W	ROS	etr_bcount	enw_bcount

Fifo occupancy ($80-$9C)

RPointer=1	0-16	Byte count FIFO 1-8	R/W	ROS	etr_bcount	enw_bcount

Parity Error ($80-$9C)

RPointer=2	0-16	Parrity Error Counter FIFO 1-8	R/W	ROS	etr_bcount	enw_bcount

Trigger Counter (low) ($80)

RPointer=3	0-16	Trigger Counter [0..15]	R/W	ROS	etr_bcount	enw_bcount

Trigger Counter (high)

RPointer=4	0-7	Trigger Counter [16..23]	R/W	ROS	etr_bcount	enw_bcount

Has unlock control) ($80)

RPointer=5	0	Mask when HAS_UNLOCK	R/W	ROS	etr_bcount	enw_bcount