Ciemat Centro de Investigaciones Energéticas, Medioambientales y Tecnológicas

ROS-8 User Manual

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PRELIMINARY

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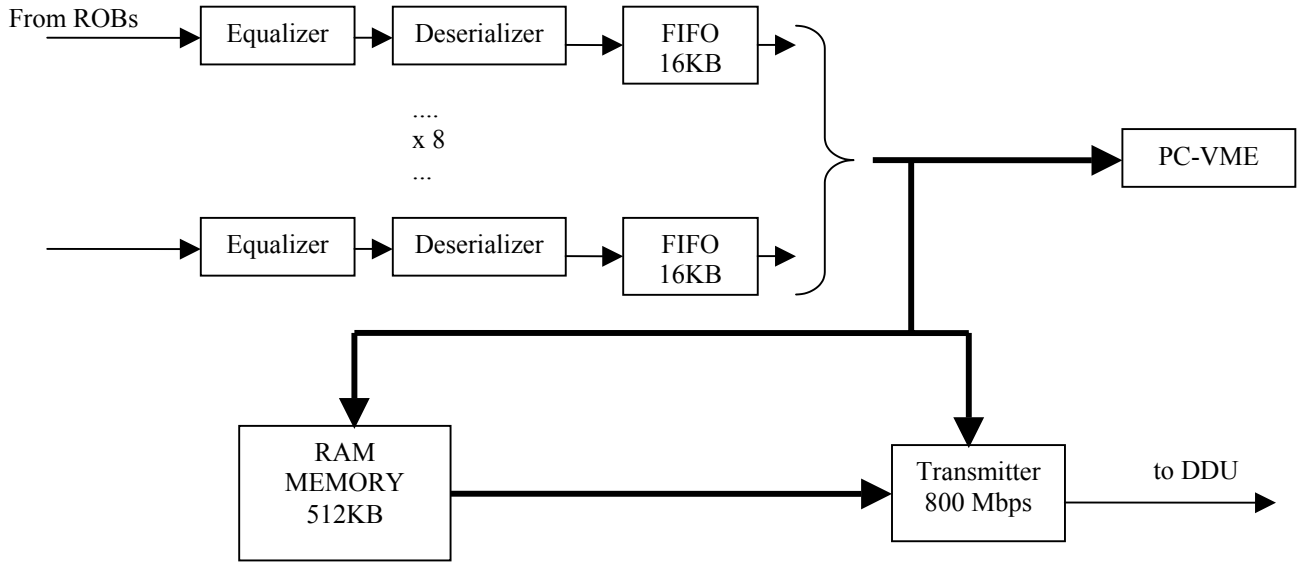
In this manual it is explained the basic functionality of the Read-Out Server (ROS) prototype with 8 input channels, developed in the CIEMAT (Madrid) for Minicrate data reading.

This is a 6U VME board with RJ-45 input and output connectors, that allows reading of up to 8 Read-Out Boards (ROBs).

In this document version, the purpose is to explain the operation mode when data is going to be read through a VME module.

1 ROS Description

In the following diagram it can be seen a scheme of the ROS data path.

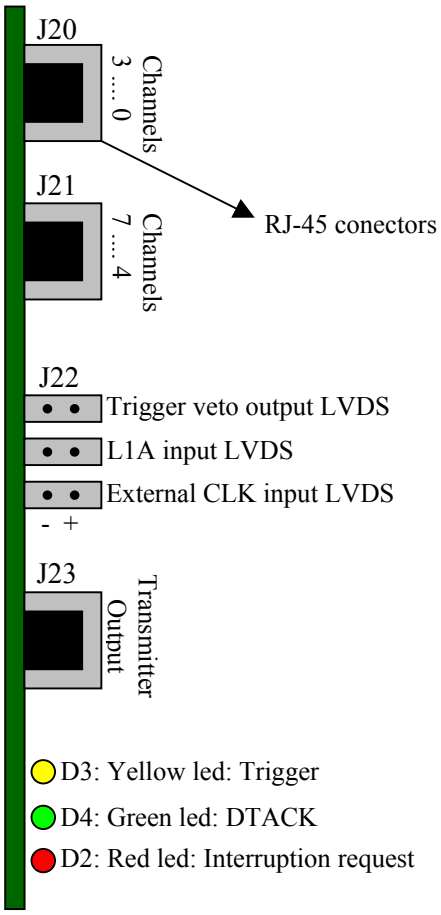


Input channels go through an equalizer that performs high-speed data recovery, and then the DS90LV1212 deserializer sends the 8 data bits plus a parity bit to the appropiate FIFO (IDT72V263) where data are stored.

There is one 16 KBytes FIFO for each channel, and they transmit their data to a common bus. Data can be read directly from the FIFOs through VME or stored in the 512Kbytes RAM memory or sent out through a Ethernet Slow (800Mbps) 8B/10B serializer.

2 ROS Connections

In the following diagram the input and output connectors of the ROS are shown:



Besides the three frontal leds that inform of the DTACK signal, Interruption request and Trigger signal, there are additional SMD leds in the board with the following purpose:

- D6: green led. Indicates the proper operation of the power supply circuitry. Whenever it is flashing it indicates a shortcircuit or any other circumstance for a high current consumption.
- D1: red led. Indicates correct programing of the U9 FPGA.
- D34, D26, D18, D14, D22, D30, D38, D10: red leds. Indicate the lock state of the deserializer. They shall turn on when the ROB is connected to the ROS and a valid code for clock recovery is being transmitted.

The jumper J16 selects between an external (J22 input) or an internal 40MHz clock:

- pin 2 connected to pin 1: internal clock
- pin 2 connected to pin 3: external clock.

There is also a switch S2 to select the U9 FPGA mode of configuration that shall be set to 0000 for configuring from the EEPROM. Push button S3 allows reprogramming of the U9 FPGA.

3 ROS Addressing

All access to this board are A24. The base address (bits A23 to A19) of the ROS can be selected with S1 switch. At least 512KB of address space shall be reserved for this board. The access may be Word accessing or Long Word accessing depending if it is to the RAM memory or to the control registers.

3.1 Access to registers: All access are Long Word.

A summary of the control registers of the ROS is shown next. It is indicated whether it is a read-only (R), write-only (W) or read and write (R/W) register.

General Control and Status Register (Base address + $00)

0-1	00 → Interrupt Disable 01 → Enable SPAE 10 → Enable SPAF 11 → Enable End of Memory	R/W	These 2 bits select and enable the source for interruptions.
2	Serializer Power Up	R/W	Enables the operation of output serializer
3	Fifo to Serializer	R/W	Enables fifo data to be transferred automatically to serializer
4	SPAE	R	Logical OR of all PAE flags
5	SPAF	R	Logical NAND of all PAF flags
6	Memory Done Memory to Serializer	R W	
7	Select Veto 0 → SPAE / 1 → SPAF	R/W	
8	Master Fifo Reset	W	Required prior to any FIFO's operation to set them in the appropriate operation mode
9	Partial Fifo Reset	W	Clears data FIFO's contents (only).
10	Load FIFO's Programmed Values	W	Loads contents of PAE and PAF Registers ($08 and $0C) into FIFO's internal registers
11	Board Reset	W	

The PAE and PAF flags are useful as a warning of whether the FIFO is near to be empty or near to be full. The number of words (offset) of margin before each flag is asserted, is programmable. A global flag for all FIFO (SPAE or SPAF) may be programmed to perform an interruption, allowing the execution of actions as vetting triggers or any other failsafe mechanism to avoid overflow.

Receiver Control & Status Register (Base address + $04)

0-7	Receiver Power Up 1-8	R/W	Bit"x"='1' enables FIFO from channel "x".
8-15	Receiver Lock 1-8	R/W	Unlock state of serializers. A '1' is written on bit "x" whenever channel "x" has at least once be unlocked. FIFO may be full of invalid data. These bits can only be erased from VME.

Programmed Almost Empty Register (Base address + $08)

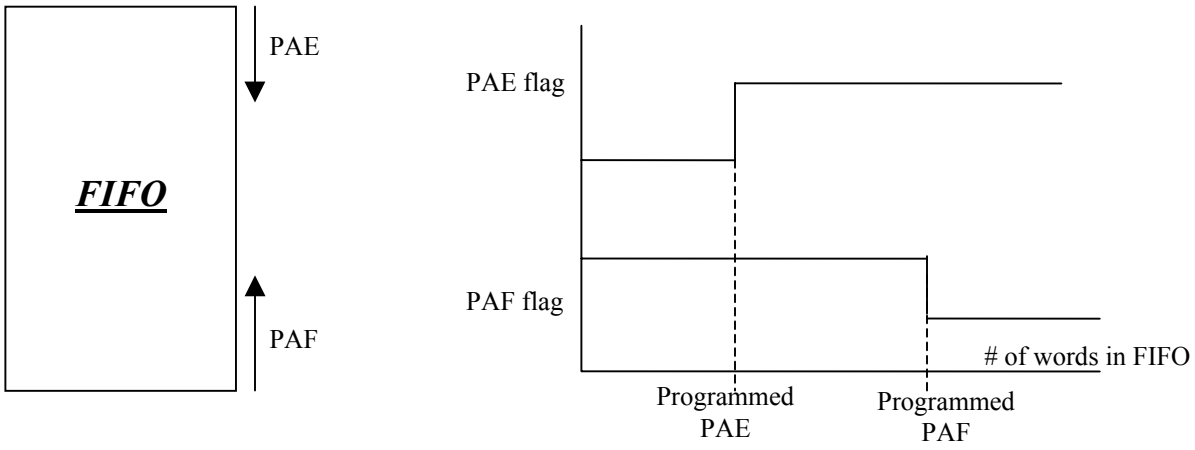
0-12	PAE	R/W	PAE value to be loaded into FIFO's registers.

The PAE value is the offset for the PAE flag, which is asserted when the number of words in the FIFO is bigger than the PAE value. PAE will be load into the FIFOs PAE registers when bit 10 from register $00 is set to '1'.

Programmed Almost Full Register (Base address + $0C)

0-12	PAF	R/W	PAF value to be loaded into FIFO's registers.

This offset represents the minimum number of empty words in the FIFO before the PAF flag is asserted. The following diagram describes PAE and PAF flags behaviour.



Fifo Full flags (Base address + $14)

0-7	FF Fifo 1-8	R	Bit "x" ='1' indicates that FIFO from channel "x" is full.
8-15	FF Latched Fifo 1-8	R	Latched values from previous flags.

PAE & PAF flags (Base address + $18)

0-7	PAE Fifo 1-8	R	PAE flags from each of the 8 FIFO´s.

8-15	PAF Fifo 1-8	R	PAF flags from each of the 8 FIFO´s.

Empty Fifo and Half Full flags (Base address + $1C)

0-7	EF Fifo 1-8	R	Empty FIFO flags from each of the 8 FIFO´s. (Active High).
8-15	HF Fifo 1-8	R	Half full FIFO flags from each of the 8 FIFO´s (Active High).

Interrupt Register (Base address + $20)

0-7	Interrupt Vector	R/W	Interrupt vector for ROS interruptions.
8-10	Interrup Level 1-7	R/W	Interrupt level for ROS interruptions.

FIFO Data Registers (Base address + $40-$5C)

0-15	Fifo 1-8 Data 0-15	R	16-bit word of data.
16	Fifo 1-8 Parity Error	R	Calculated and received does not match.
17	Fifo 1-8 Parity 0	R	Received parity of least significant byte from data.
18	Fifo 1-8 Parity 1	R	Received parity of most significant byte from data.
19	Fifo 1-8 EF	R	Empty FIFO flag at the moment of reading.
20	Fifo 1-8 FF	R	Full FIFO flag at the moment of reading.
21	Fifo 1-8 PAE	R	PAE flag of this FIFO at the moment of reading.
22	Fifo 1-8 PAF	R	PAF flag of this FIFO at the moment of reading.

Each of this registers correspond to each of the FIFOs, that is $40 to FIFO 0, $44 to FIFO 1, ...

Each access to these registers performs a new read cycle of the next FIFO word, until the FIFO is empty. Since then, the EF flag will be asserted and the data output will remain at the last read value.

PAE & PAF programmed values (Base address + $60-$7C)

0-12	PAE / PAF Values FIFO 1-8	R	Read Sequentially PAE & PAF FIFO Values

Each of this registers correspond to each of the FIFOs, that is $60 to FIFO 0, $64 to FIFO 1, ... The value read is the stored PAE and PAF value in each FIFO, sequentially one after the other. First access to these registers does not give a valid value. In order to read properly PAE and PAF values, four accesses have to be done each time.

4 VME Mode of Operation

In this mode of operation data is read through the PC with an VME access, but they are not sent to the memories nor the serializer. Notice that this will require a different mode of operation and data will probably have a different format.

4.1 ROS configuration

a) Reset the ROS (0x800 -> $00)
b) Master FIFO reset (0x100 -> $00)
c) Optional: Write PAE value (PAE -> $08) (Default offset: 511 words)
d) Optional: Write PAF value (PAF -> $0C) (Default offset: 511 words)
e) Optional: Load PAE and PAF values in the FIFOs (0x400 -> $00)
f) Enable FIFOs (For example, if you want to enable channels 7, 4, 1 y 0, you write "10010011" -> $04)
g) LOCK reset: Once enabled the channels it is necessary to erase the old latched values of lock. Write "00XX" -> $04. Where XX is the value written in step f).
h) Check the LOCK value: Read most significant byte from $04.
i) Optional: Check PAE and PAF loaded values: Read four times from register $60+4*ROS channel. First value is invalid, next value is PAE and next is PAF. Ignore last value.

4.2 Reading from ROS

a) Read sequentially from the register $40+4*ROS channel until bit 19 turns to 1. This last value when EF='1' is not valid, it is the same value that has already been read.
   Parity errors can be monitorized (bit 16) and re-checked, comparing them with bits 17 and 18. FF, EF, PAE and PAF can be monitorized also when desired.

The format of the incoming data is the same as if they were read directly from the TDC [1] but one 16-bit word at a time (most significant word first). Next it is shown an example of a normal data flow where there is one readout event with five hits.

Words	
300	TDC Master = 3 Event ID = 0 Bunch ID = 2775
AD7	
4000	TDC = 0 Channel = 0 Time (ns) = 371
76C	
4060	TDC = 0 Channel = 12 Time (ns) = 370
768	

4008	TDC = 0 Channel = 1 Time (ns) = 371
76C	
4010	TDC = 0 Channel = 2 Time (ns) = 371
76C	
4018	TDC = 0 Channel = 3 Time (ns) = 371
76C	
1300	TDC Master = 3 Event ID = 0 Wordcount = 7
7	
300	TDC Master = 3 Event ID = 1 Bunch ID = 87
1057	
....	.....

5 References

[1] "High Performance Time to Digital Converter". Version 2.1. J. Christiansen. CERN/EP – MIC. July 2002. Accesible from:

http://micdigital.web.cern.ch/micdigital/hptdc/hptdc_manual_ver2.1.pdf