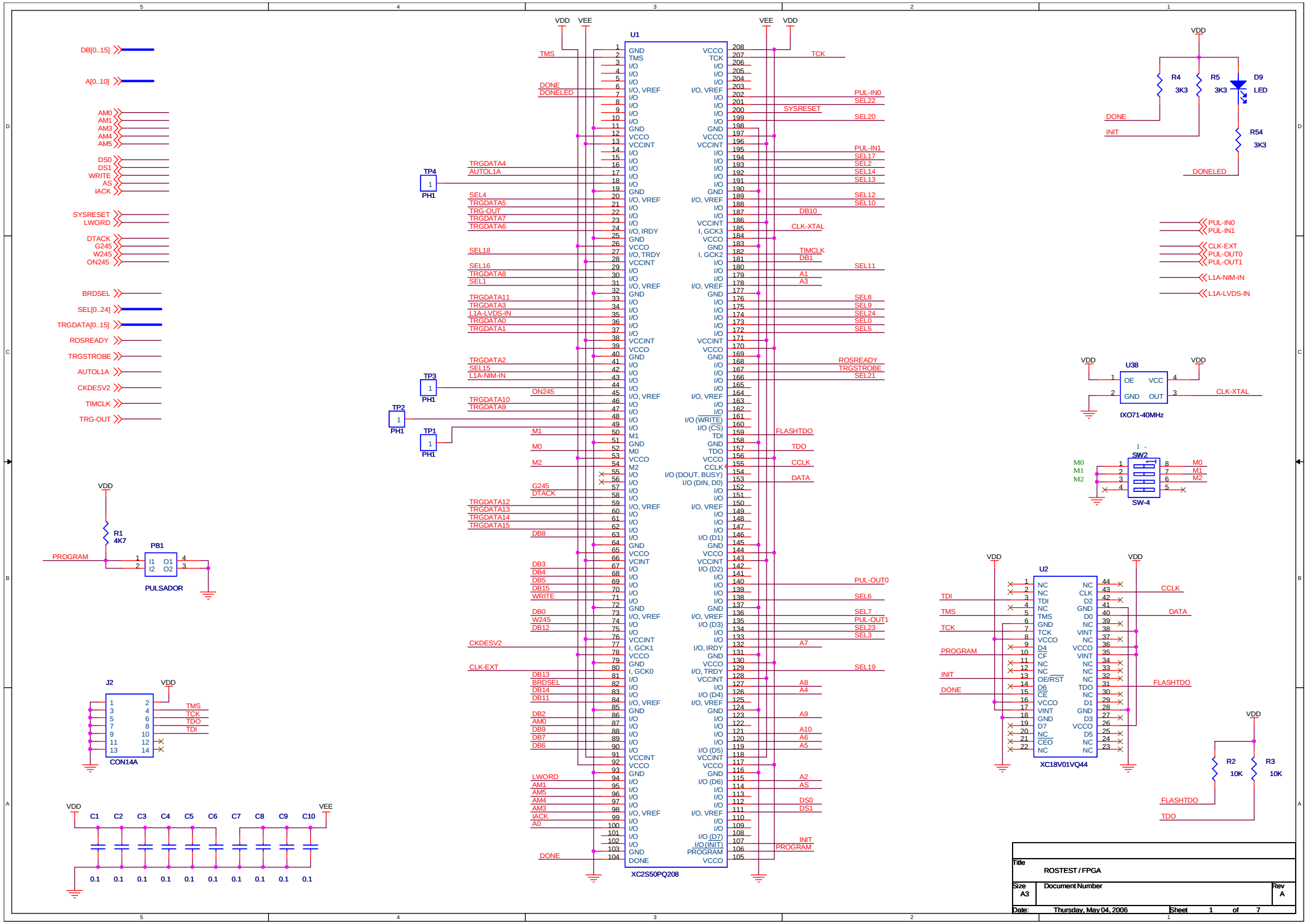
U1
XC2S50PQ208
U2
XC18V01VQ44
U38
IXO71-40MHz
SW2
SW-4
PB1
PULSADOR
J2
CON14A
TP1
TP2
TP3
TP4
PH1
R1 4K7
R4 3K3
R5 3K3
D9 LED
R54 3K3
R2 10K
R3 10K
C1 C2 C3 C4 C5 C6 C7 C8 C9 C10
0.1
VDD
VEE
DB[0..15]
A[0..10]
AM0
AM1
AM3
AM4
AM5
DS0
DS1
WRITE
AS
IACK
SYSRESET
LWORD
DTACK
G245
W245
ON245
BRDSEL
SEL[0..24]
TRGDATA[0..15]
ROSREADY
TRGSTROBE
AUTOL1A
CKDESV2
TIMCLK
TRG-OUT
PROGRAM
DONE
INIT
DONELED
PUL-IN0
PUL-IN1
CLK-EXT
PUL-OUT0
PUL-OUT1
L1A-NIM-IN
L1A-LVDS-IN
CLK-XTAL
FLASHTDO
TDO
CCLK
DATA
TDI
TMS
TCK
M0
M1
M2
Title
ROSTEST / FPGA
Size
A3
Document Number
Rev
A
Date:
Thursday, May 04, 2006
Sheet
1
of
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