Ciemat Centro de Investigaciones Energéticas, Medioambientales y Tecnológicas

TIM User Manual

Version 1.0

J.M. Cela, C. Fernández, C. Willmott.

Electrónica y Automática.
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1 Introduction

The TIM board is a 9U VME board used for interface between the TTC system and the Sector Collector crate, that is, the Sector Collector boards and the ROS-25 boards.

It is made up of different boards:

1) A TTCrq board, which contains the optical receiver for the TTC optical link and a TTCrx ASIC that decodes the TTC signals.

2) A TIM-TTC board that receives the signals from the TTCrx and stores the necessary information that can be read from VME accesses. It also allows configuration of the TTCrx through an I2C interface.

3) A TIM-VME board which mainly handles the VME access.

4) A TIM-LED board for visualization of the TIM board status.

In the following pages a picture of the board with its main elements is shown, and it is also presented the front-panel of the TIM with the meaning of the different leds.

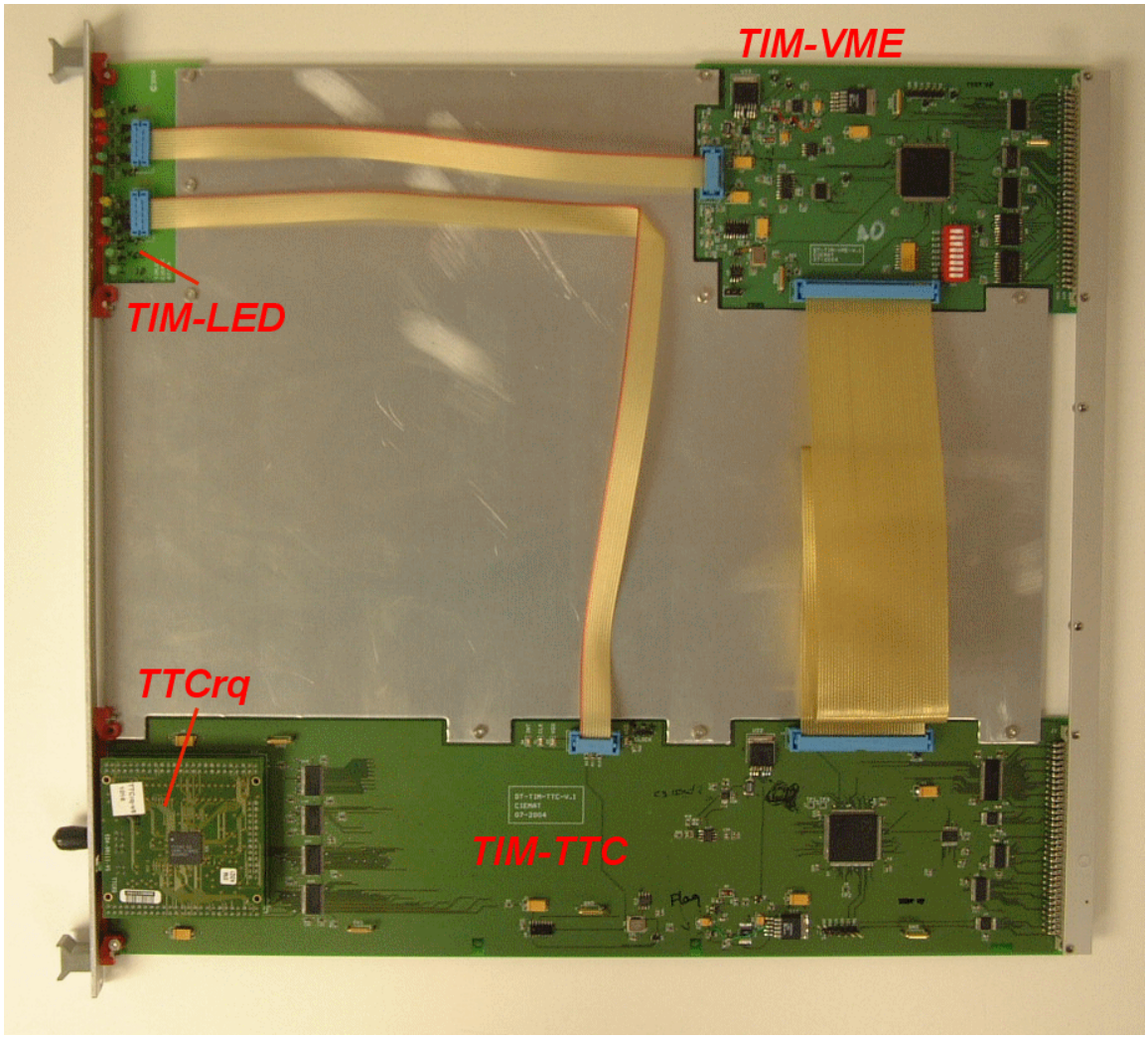
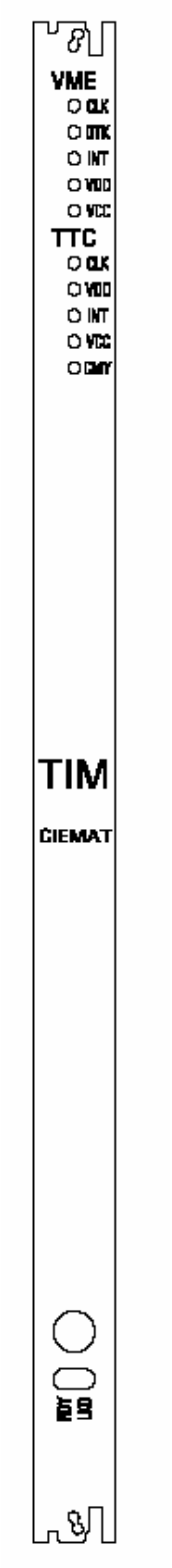


Figure 1: TIM board.



VME

CLK: ON = clock is received from TIM-TTC
DTK: ON = VME data transfer acknowledge
INT: ON = interruption requested
VDD: ON = 3.3V power on
VCC: ON = 5V power on.

TTC

CLK: ON = clock is received from the TTCrq board.
VDD: ON = 3.3V power on
INT: ON = interruption requested
VCC: ON = 5V power on
CMY: spare

TTC optical fiber input.

RDY: ON = TTCrx ready.
LKD: ON = QPLL locked.

The QPLL is only locked at the LHC frequency. Note that this is not the frequency that the TTCex module generates.

Figure 2: TIM front pannel.

2 VME Interface

TheVME interface to the TIM board is performed through standard A16 access 16 bit words. The address selection is done through switch S1. At this moment the TIM board base address is A100.

In what follows it is explained the content of the different registers. The default value corresponds to the expected proper value read after a reset.

2.1.1 Register $00 Default value = 0x04

General Control & Status

2	ttc_on	R	1 = the TIM-TTC board is connected.
3	was_off	R/W	1 = At some point the TIM-TTC board has been disconnected.
15	global board reset	W	It resets all TIM board except for the TTCrq board.

2.1.2 Register $40 Default value = 0x01

TTCrx Control & Status

0	TTCrx ready	R	1 = The TTCrx is connected and ready.
1	sinerr_str	R	Single error at the TTCrx. (See manual).
2	dberr_str	R	Double error or frame error at the TTCrx. (See manual).
14	reset I2C chip	W	
15	TTCrx reset	W	When writing a 1, a reset is sent to the TTCrq board.

2.1.3 Register $46 Default value = 0x00

BCNT register

0-11	Bunch counter	R

It stores the Bunch counter value sent from the TTCrx after each L1A.

2.1.4 Register $48 Default value = 0xFFF

EVCNTL register

0-11	Event counter low	R

It stores the 12 least significant bits of the Event counter value sent from the TTCrx after each L1A. After an Event counter reset, the first L1A is signalled with an Event counter value of 0.

2.1.5 Register $4A Default value = 0xFFF

EVCNTH register

0-1	Event counter high	R

It stores the 2 most significant bits of the Event counter value sent from the TTCrx after each L1A. After an Event counter reset, the first L1A is signalled with an Event counter value of 0.

2.1.6 Register $4C Default value = 0x01

QPLL Control & Status

0	QPLL locked	R	1 = the QPLL is locked
1	QPLL error (SEU)	R	1 = an SEU error from the QPLL
2-9	SEU counter	R	It counts the amount of SEU errors from the QPLL
14	Reset SEU counter	W	
15	Reset QPLL	W	

The QPLL is only locked at the exact LHC frequency. Note that this is not the one that provides the TTCex.

2.2 I2C Interface with the TTCrx

The configuration registers of the TTCrx can be read or written through an I2C interface. The VME to I2C interface is performed through the device PCA9564, based on a protocol that uses four registers. The access to this registers is performed by accessing to the following VME registers:

2.2.1 Register $88

I2C-0 Status

0-7	Status	R	Default value = 0xF8
0-7	Time-out	W	Default value = 0xFF

2.2.2 Register $8A Default value = 0x00

I2C-0 Data

0-7	I2C Data	R/W

2.2.3 Register $8C Default value = 0x00

I2C Own adress

0-7	I2C address	R/W

2.2.4 Register $8E Default value = 0x00

I2C-1 Control

0-7	I2C control	R/W

More detailed information of the I2C access will be included in following versions of this document and it can also be found in the given references.

Note:

The address of the TTCrx chip, indicated with a label at the TTCrq board, is set at power up through some resistors at the TTCrq board. At the moment the address is ID = 06.

3 Configuration

After power up it is recommended to execute a reset of the board (write 0x8000 at register Base Address + 0x00) and a reset of the TTCrq (write 0x8000 at Base Address + 0x40).

Therefore, the board will be ready to operate. It is recommended to check that the TTCrx is ready (bit 0 of register Base Address + 0x40) and that the QPLL is locked and there are no SEU errors. (register Base Address + 0x4C).

4 References

1) TTC system. http://ttc.web.cern.ch/TTC/intro.html

2) TTCrx reference manual. http://ttc.web.cern.ch/TTC/TTCrx_manual3.11.pdf

3) QPLL ASIC. http://proj-qpll.web.cern.ch/proj-qpll/

4) TTCrq. http://ttc.web.cern.ch/TTC/TTCrqSpec.pdf

5) PCA9564 datasheet.
http://www.semiconductors.philips.com/pip/PCA9564N.html