Control-X is a VME multipurpose board designed to operate Readout Boards (ROB's) under all possible circumstances.

It includes:

- Trigger synchronization, delay, counting, generation through VME, and interfaces with several common standards.
- Two test pulse handling with independent delays, and pulse generation via VME.
- Interrupt generation: externally from two different sources, or internally at the end of a programmable trigger count.
- Full ROBUS operation.

40 MHz Clock

The clock to operate the board can be selected through a jumper (see Fig. x) from an on boards quartz, and external NIM input, or an external TTL input. The selected clock is output at the front panel: LVDS OUT CLK0..7 and LVPECL OUT CLK.

Trigger handling

All trigger sources are merged into one common internal trigger signal. This signal is output as LVDS OUT T0 in the front panel. Then it is synchronized with the 40 MHz clock and fed into the shift delay line. The selected outputs of the shift delay line (Reg. $02) are OR-ed and send to the various trigger outputs (NIM OUT TRG, LVPECL OUT TRG, LVDS OUT TRGSY, and ROBUS trigger line) only when
a) trigger count bypass is selected: bit_3 in Reg. $00 set to 0 or
b) trigger count bypass is de-selected (previous bit ser to 1) and trigger count has not reached the programmed trigger max count (Reg. $04).

Trigger counting

When the trigger counting option is selected by setting bit_3 in Reg. $00 to 1 and a programmed trigger count is written into Reg. $04, this number of triggers is sent to the various trigger outputs. After that, trigger output is stopped and subsequent arriving input triggers are counted in Reg. $0E + $0C (Trigger_Count_Out). A new sequence can be restarted by writing a 1 in bit_8 Reg. $1E. At that moment Trigger_Count_Out register is reset and its contents is transferred to Trigger_Count_Out_Latch ($0A + $08).
A high level on input IN VETO also stops triggers being send to output connectors and initiates Trigger_Count_Out mechanism.

Test pulses

Test pulses can be generated through VME (bit_4 and bit_5 in Reg $1E) or via front panel connectors: TTLIN PLS0, TTLIN PLS1. After a programmable delay (Reg $16 and Reg $18) pulses are output on front panel connectors LVDS OUT PLS0 and LVDS OUT PLS1.

Interrupts

Interrupts can be generated via two independent front panel input connectors, NIM IN INT0 and NIM IN INT1, or at the end of Trigger_Count_In. All three interrupts have independent registers ($10, $12 and $14) to select interrupt levels and vectors. In addition Interupt_0 and Interupt_1 can be programmed to accept:
a) Polarity: active low or active high (bit_11)
b) Pulse: level or edge (bit_12)
c) Source (input Lemo connector): LVDS OUT PLS0 and LVDS OUT PLS1.

ROBUS

A 40-pin Yamaishi connector interconnects to all ROBUS signals. More specifically:
a) Reg $1A: 7 ROB ON signals
b) Reg $1C: JTAG interface
c) Reg $1E, in addition to trigger signal it provides: Bunch_Counter_Reset, Reset, Event_Reset, Test_Mode_Advance, and Test_Mode_Reset. The signal Test_Mode is implemented in bit_4 Reg $00.
d) Reg $20, $22, $24, and $26: TDIO bus interface

Control_X Registers

All access A16

Register Access (Standard)

Register 0 ($00) G0.0

General Control & Status

0	enable external interrupt 0	R/W	
1	enable external interrupt 1	R/W	
2	enable end_count (interrupt 2)	R/W	
3	trigger count bypass	R/W	0=bypass
4	enable test mode (track)	R/W	
5	ROB power fault latch	R/W	1=fault
6	ROB power fault	R	
7	ROB error	R	1=error
8	interrupt requested 0	R	
9	interrupt requested 1	R	
10	trigger end count	R	
11	board global reset	W	

Register 1 ($02) G0.1

Trigger delay

0-15	trigger shift delay (200ns step; max 3.2 us)	R/W

Register 2 ($04)G0.2

Trigger max count

0-14	trigger max count	R/W
15	trigger end-count interrupt	R/W

Register 3 ($06) G0.3

Trigger count in

0-15	trigger count in	R/W

Register 4 ($08) G1.0

Trigger count out latch 0

0-15	trigger count out latch 0-15	R

Register 5 ($0A) G1.1

Trigger count out latch 1

0-15	trigger count out latch 16-31	R

Register 6 ($0C) G1.2

Trigger count out register 0

0-15	trigger count out register 0-15	R/W

Register 7 ($0E) G1.3

Trigger count out register 1

0-15	trigger count out register 16-31	R/W

Register 8 ($10) G2.0

Interrupt 0

0-7	Interrupt Vector_0	R/W
8-10	Interrup Level_0 (1-7)	R/W
11	Polarity_0	R/W
12	Pulse_0	R/W
13	Select Lemo0/Lemo1	R/W

Register 9 ($12) G2.1

Interrupt 1

0-7	Interrupt Vector_1	R/W
8-10	Interrup Level_1 (1-7)	R/W
11	Polarity_1	R/W
12	Pulse_1	R/W
13	Select Lemo1/Lemo0	R/W

Register 10 ($14) G2.2

Interrupt 2 (end_count)

0-7	Interrupt Vector_2	R/W
8-10	Interrup Level_2 (1-7)	R/W

Register 11 ($16) G2.3

Pulse 1 delay

0-6	Delay 0.5ns step (max 64 ns)	R/W
7-13	Delay 25 ns step (max 3200 ns)	R/W

Register 12 ($18) G3.0

Pulse 2 Delay

0-6	Delay 0.5ns step (max 64 ns)	R/W
7-13	Delay 25 ns step (max 3200 ns)	R/W

Register 13 ($1A) G3.1

ROB on_off register

0	RON 0	R/W
1	RON 1	R/W
2	RON 2	R/W
3	RON 3	R/W
4	RON 4	R/W
5	RON 5	R/W
6	RON 6	R/W

Register 14 ($1C) G3.2

JTAG

0	JTCK	R/W
1	JTMS	R/W
2	JTDI	R/W
3	JTADD0	R/W
4	JTADD1	R/W
5	JTADD2	R/W
6	JTADD3	R/W
7	JTDO	R

Register 15 ($1E) G3.3

ROB pulse register (25 ns)

0	Bunch Counter Reset	W
1	Trigger	W
2	Reset	W
3	Event Reset	W
4	Pulse 1 (50 ns)	W
5	Pulse 2 (50 ns)	W
6	test mode advance	W
7	test mode reset	W
8	set trigger count in	W

Register 16 ($20) G4.0

TDIO write

0	Bit to be writen	R/W

Register 17 ($22) G4.1

TDIO read

0	Bit read during last command	R

Register 18 ($24) G4.2

TDIO command

0	Initialization command	W
1	Write command	W
2	Read command	W

Register 19 ($26) G4.3

CRC

0-7	CRC register	R/W