Technical Information

Model 365A/365AL

Dual Four-Fold Logic Unit

WARRANTY

All LRS instruments are guaranteed to operate within their specifications for one year from the date of purchase. Under this warranty, any unit which fails to perform within specifications, as a result of defects in workmanship or materials, will be restored to specified operating condition free of charge except for shipping costs involved in the return of the unit to the factory.

In order that this warranty be considered valid, it is necessary that the LRS Warranty Card which accompanies the unit on delivery be completed and returned to the factory within 30 days of receipt of equipment.

All questions concerning repairs or replacement parts should be addressed directly to factory's Quality Control Manager. This procedure will insure the fastest possible service. Please include the model type and serial number with all requests for parts or service.

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GENERAL DESCRIPTION

The Model 365A and 365AL are dual 4-fold logic units which offer the functions of fan-in, coincidence, leading edge inhibit, majority logic, and pulse standardization. Each of two identical channels accepts standard NIM logic signals at each of the four logic inputs and one veto input. All inputs are terminated in 50Ω. Lemo-type connectors are used with the single-width Model 365AL; BNC type connectors are used with the double-width Model 365A.

A front-panel selector allows programming the number of simultaneous negative inputs required for an output. With its majority logic capability, the unit may be used to perform voter coincidence such as 1 of 1,2,3,4 (logic fan-in), 2 of 3,4, or 3 of 4 as well as the standard coincidences of 2 of 2, 3 of 3, 4 of 4. Any of the inputs serves as an inhibit input when driven with a complementary logic signal. A separate veto input is provided for inhibiting the output regardless of the state of other inputs. This veto signal need only overlap the leading edge of the coincidence in order to inhibit the output.

Both channels of the 365A/365AL may be gated off by means of the NIM bin gate. The bin gate enters the module via the rear multipin power connector and a rear-panel On-Off switch. Quiescently at +5 volts, the bin gate must be clamped to ground to inhibit the logic unit. The bin gate is direct-coupled, and has rise and fall times of approximately 50 ns.

A front-panel selector is provided for programming the participating inputs. Inserting the programming pins in any of the designated Off positions disables that input and eliminates the necessity of removing input cables. A separate storage location is provided for holding the programming pins not in use.

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October 1972

Once the input coincidence conditions have been satisfied, the Model 365A, 365AL generates three double-amplitude NIM fast logic outputs. Each output is provided with two paralleled connectors to enable the signal to be clipped, back-terminated, or fanned-out to two 50 Ω loads. The positive output, or complement (OUT), is quiescently at a logical one state (-32 mA) and switches to 0 mA (or 0 volts) for the duration of the output. The two negative outputs (OUT) are quiescently at zero and switch to -32 mA (-800 mV if both connectors drive 50Ω loads) during an output.

The output duration of each channel is adjustable by means of a front-panel potentiometer from 3.5 ns to 50 ns.

The Model 365A/365AL, is a deadtimeless circuit and will respond to input signals even when an output is already present. The minimum pulse pair separation is under 6 ns for an equivalent CW rate of greater than 150 MHz. If a second coincidence is detected during the time the output from a first coincidence is being produced, the unit will extend the output duration to reflect the occurrence of the second signal. The net output pulse, being the logical sum of two standard output pulses, is of standard amplitude and retains the time information contained in the input signals.

The Model 365A/365AL offers non-multiple-pulsing operation to assure unambiguous response to input pulses regardless of their amplitude or duration. The 365A/365AL will not produce multiple pulses even with input pulses that substantially exceed the output pulse in duration.

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SPECIFICATIONS

Number of Channels: Two, all identical.

Input Levels: NIM logic levels: logical 0, 0 mA ± 2 mA; logical 1, 16 mA ± 2 mA.

Input Impedance: 50 Ω ± 5%; value of impedance is constant up to the limit of input protection for negative inputs.

Input Protection: ± 5 volt protection for pulses. DC overload characteristics are determined by the 250 mW dissipation limit of the 50 Ω input terminating resistor.

Input Coupling: Direct; coupling is independent of input risetime, duration, and rate.

Input Reflections: Dependent upon input risetime; less than 10% for input signal of 2 ns risetime or greater.

Gate: Logic unit may be inhibited by application of NIM Bin Gate. Bin Gate enters module via pin of rear multipin connector. Switch located on back panel disconnects 365 from Bin Gate line. Clamping Bin Gate to ground from + 5 volts inhibits. Clamping circuit must sink 3 mA per module. Bin Gate circuit is direct-coupled. Rise and fall times are 20 ns.

Negative Outputs: Two, both with paralleled connectors driven by common high impedance current source. Quiescently, 0 mA, current source switches to - 32 mA during output.

Positive Output: One, complementary, paralleled connectors, quiescently - 32 mA (- 1.6 mV into 50 Ω load), switching to zero volts during an output.

Output Duration: 4ns FWHM to 50 ns, continuously adjustable by means of front-panel width control.

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Output Rise and Fall Times: 1.2 ns typical, 10% to 90%; fall time slightly longer on wider widths.

Output Duration Stability: Less than 0.1%/° C from 20° C from 60° C.

Coincidence Width: 1 ns up, determined by input pulse duration.

Double Pulse Resolution: Minimum separation to resolve two pulses is typically under 6 ns.

Maximum Rate: 160 MHz typical, input and output; defined for input signals of -600 mV, 3.5 ns FWHM.

Functions: ANDing, ORing, Majority, Inhibit and Complementary logic.

Input-Output Delay: 8.0 ns ± 5% channel-to-channel variation; jitter <20 ps rms.

Counting Efficiency: Deadtimeless operation; recovery time is less than output pulse duration; there is no deadtime following output pulse at output durations greater than 8 ns; output duration will update to reflect new input if retriggered while output pulse is present.

Multiple Pulsing: None; one and only one output is produced for each input pulse regardless of input pulse amplitude or duration.

Power Requirements: 8.8 watts total; +12 volts at < 120 mA, -12 volts at 160 mA, 120 VAC at 33 mA; voltages must be regulared to ± .1%.

Packaging: The Model 365A/365AL, are packaged in conformance with AEC standard for nuclear modules (AEC Report TID 20893 Rev.) Completely compatible physically and electrically with LRS Power Chassis Model 108P, and with any other AEC standard power bin of any manufacturer. Model 365AL is single-width module using Lemo-type connectors and Model 365A is double-width module using BNC-type connectors.

CIRCUIT DESCRIPTION

The Model 365A/365AL Dual 4 Fold Logic Unit is composed of six basic sections as indicated on the block diagram: a current switch for each input, a selectable current source to set coincidence level, a tunnel diode section to provide pulse standardization, a pulse veto section to clip or completely inhibit the tunnel diode pulse, a pulse-forming stage to provide adjustable output widths, and the output buffers.

The current switch at each input provides buffering with proper temination and On-Off control, and causes an 8.6 mA current to be subtracted from the coincidence level current for the duration of the input pulse. The current switch is composed of a MC 1664 non-inverting AND gate. The input may be disabled by shorting the second input of the gate to ground causing the signal input to be ignored. Quiescently, the output of the 1664 gate is "high" (0 volts) and is supplying the current to the 523 Ω resistor which serves as the 8.6 mA current source. An input signal level (-600 mV or greater) causes the open emitter of the output of the 1664 gate to go low, allowing the MBD-101 diode to conduct the 8.6 mA. Since the anodes of the four MBD-101's are connected as a current summing point, each input signal causes 8.6 mA to be substracted from the coincidence level current source.

The coincidence level current source supplies from 14.3 mA to 40.1 mA depending upon the coincidence level selected. In the "singles" position, the current source supplies 10 mA for the current source buffer, plus 4.3 mA, or 1/2 of an input current switch unit. Each additional level selected over a singles requirement increases the available current by 8.6 mA. The amount of current available is supplied by the collectors of two transistors connected in a Darlington configuration. The emitter of the second transistor is held at a constant voltage equal to the reference voltage generated by the coincidence level selector. The actual current is determined by the voltage across the two paralleled 432 Ω resistors at the transistor emitters. Any difference between the emitter voltage and the reference voltage is detected by the 741 operational amplifier which adjusts the Darlington input to provide the correct output. This circuit provides stable currents independent of temperature and transistor characteristics.

The tunnel diode section provides a fast-rise, fixed-amplitude pulse anytime the inputs equal or exceed the coincidence level selected. Quiescently, the tunnel diode is in its low voltage state, being supplied with approximately 8.4 mA from the 510 Ω resistor to the -5 volt supply. When the current from the input current switches exceeds that which is available from coincidence level current source, the voltage at the current summing junction drops. This is transmitted through the differential stage (Q3, Q4) to the 10 mA tunnel diode, causing the tunnel diode to switch to its high voltage state. This in turn allows IC A B pin 14 to switch to its positive state. This transition is passed onto the next section of IC A B through the 43 ohm resistor, in addition to driving a 2 ns printed circuit delay line. After the 2 nsec delay the emitter of Q5 is switched from approximately -1.5 volts to -.8 V thereby back biasing the FD777 diode allowing the current in the tunnel diode to drop to a level just sufficient to keep the diode in its high voltage state. When the input coincidence condition is removed the differential stage switches back to its quiencient state and allows the T.D. to switch back to its low level state.

The output of the delay line also drives one input of the veto gate I.C. A B (pins 12,13 & 15), which provides a delayed signal at its output. The overlap of the normal and delayed signals cause I.C. A B 3 to provide a 2 nsec wide current pulse which is independent of the duration of input signal overlap. If either a veto input signal or a bin gate level is present during the 2 nsec overlap the overlap will be ignored and no output will be generated. The 2 nsec current pulse is supplied to the pulse forming section which generates the desired width output pulse.

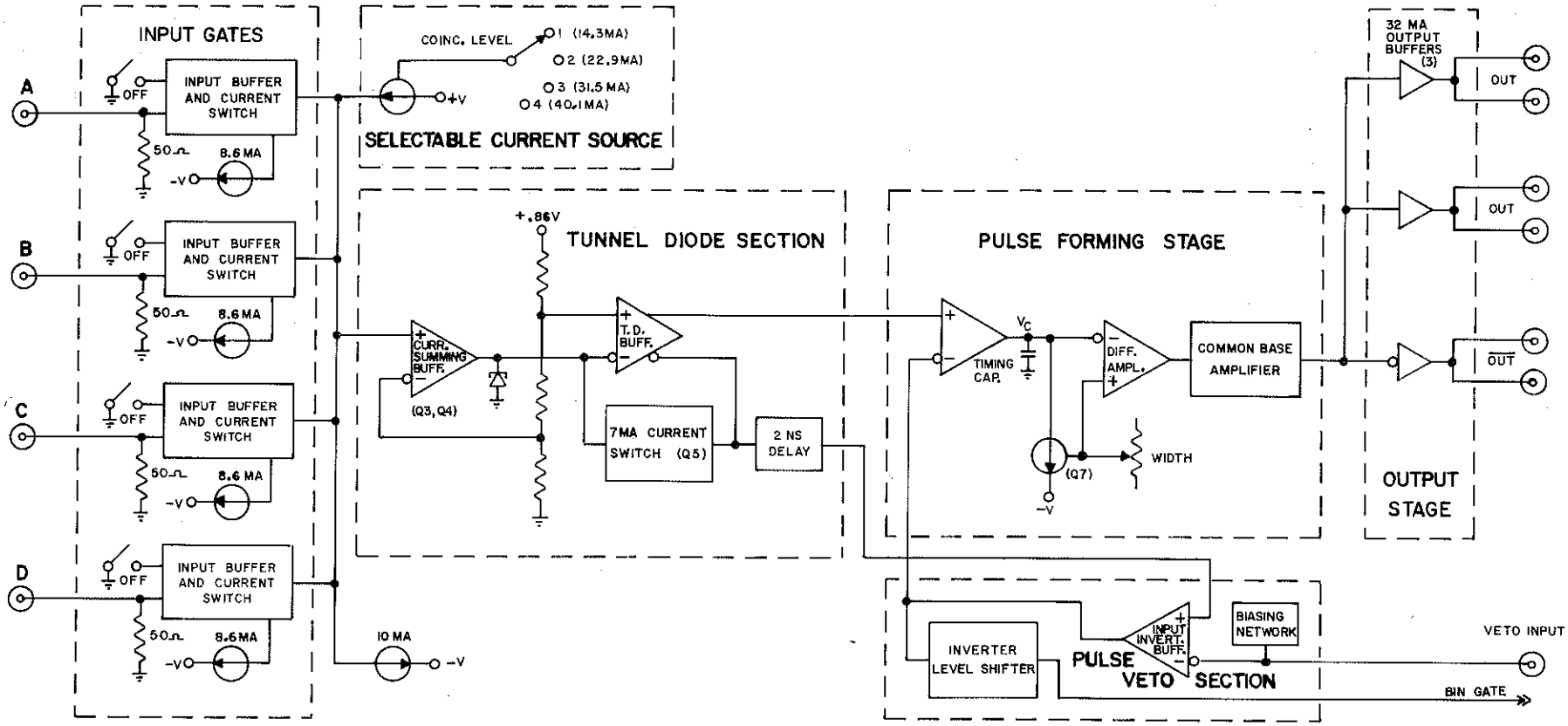
The pulse-forming section, each time a current pulse is received, generates a standardized pulse with a width that is set by the front-panel 2 KΩ width potentiometer. The actual width is determined by a ramp and a comparator. The ramp is generated by raising a capacitor to a fixed voltage using the output of IC A B pin 3, and discharging it with an adjustable current source. The comparator is composed of the last section of IC A B which generates an output signal whose width is equal to the amount of time the ramp is above an adjustable threshold. The threshold and the adjustable current source are both determined by the front-panel-mounted width potentiometer. Coupling the threshold and ramp slope in this manner permits stable control of the output width over a 4.0 - 50 ns range. Deadtimeless operation is inherent in this design because anytime a pulse is received at IC A B pin 3, the

capacitor is again raised to the initial rundown voltage. The resulting output thus reflects the receipt of the additional coincidence by extending the output width.

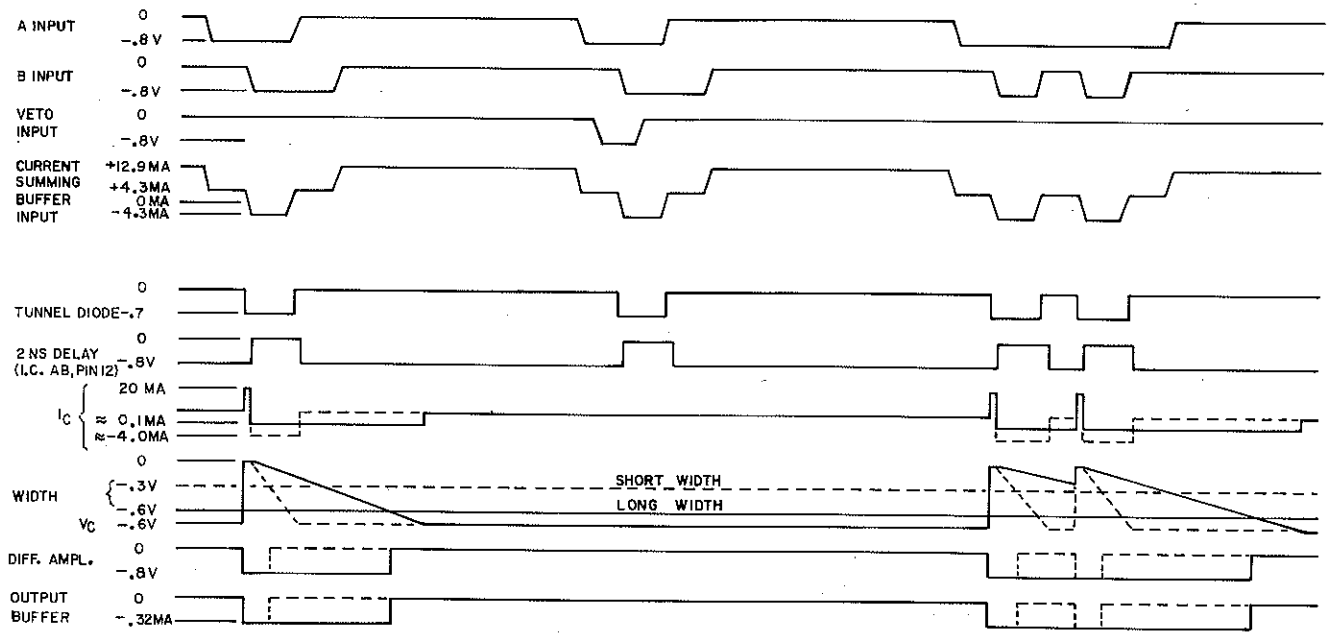
The output buffers provide 32 mA current source output pulses with widths determined by the pulse-forming stage. The output of the comparator drives a common base amplifier stages. Quiescently, each output buffer stage is balanced with one transistor "on" and one transistor "off". The "on" transistor of one stage is connected to the complementary output, which is quiescently at 32 mA, switching to 0 mA during an output. The "off" transistors tied to the normal (OUT) connectors quiescently supply 0 mA and switch to 32 mA during an output. Each output drives two paralleled connectors. All outputs limit at approximately 2 volts.

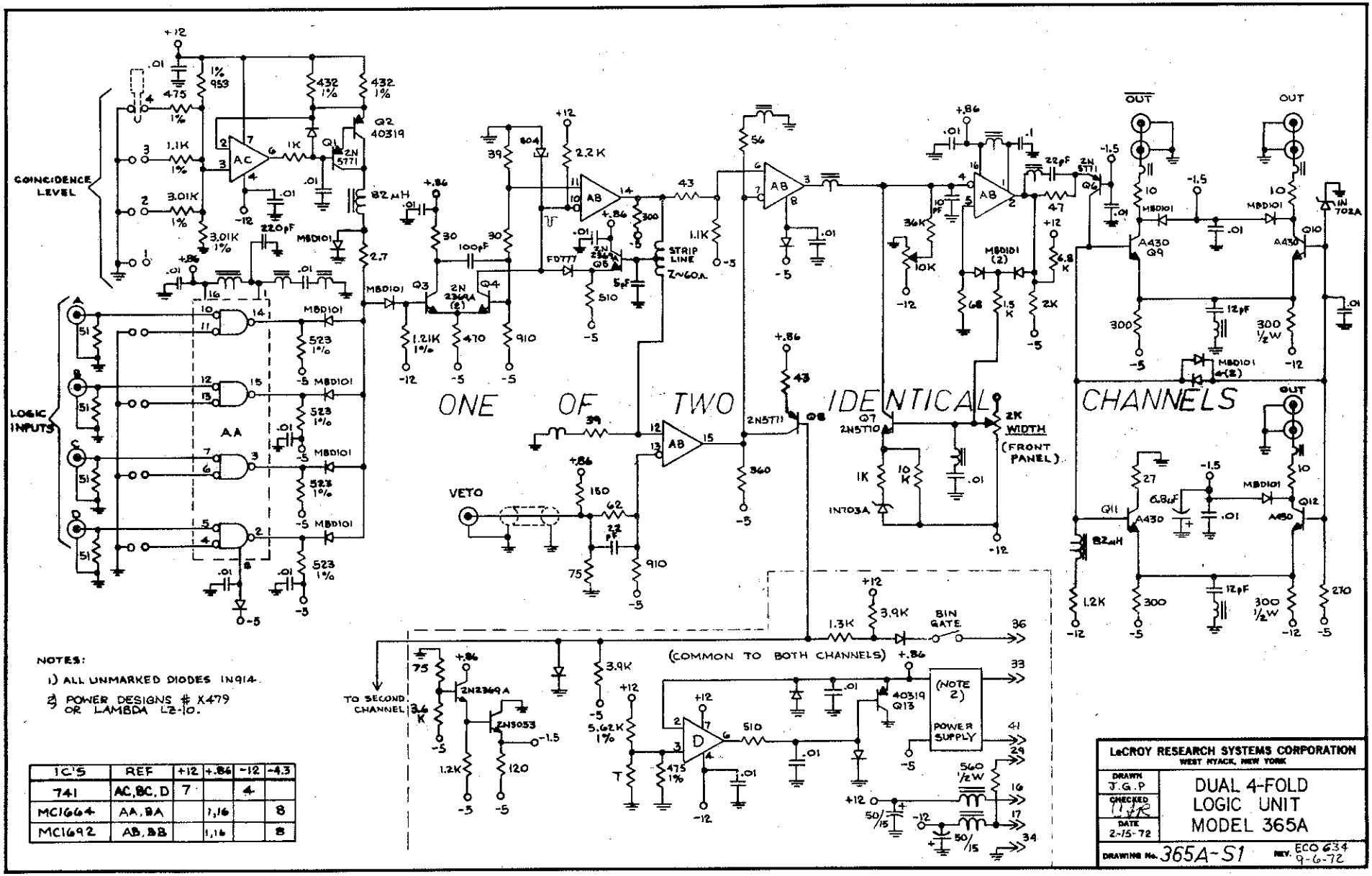
In addition to using the standard ±12 volts from the power connector, the Model 365A/365AL, also requires + 0.8 and -5.0 volts. This is supplied by an internal 5.8 volt supply using 120 VAC from the rear power connector. The positive side of the supply is referenced to +0.8 volts by an emitter follower operating from a 741 operational amplifier. The reference for the op-amp is derived from a resistor divider connected between + 12 volts and ground.

MODEL 365 BLOCK DIAGRAM



INTERNAL WAVEFORMS USING TWO INPUTS – A & B, WITH COINCIDENCE LEVEL SET AT 2.





IC'S	REF	+12	+.86	-12	-4.3
741	AC, BC, D	7		4	
MC1664	AA, BA		1,16		8
MC1692	AB, BB		1,16		8

LeCROY RESEARCH SYSTEMS CORPORATION
WEST NYACK, NEW YORK

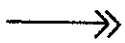
DRAWN J.G.P	DUAL 4-FOLD LOGIC UNIT MODEL 365A
CHECKED	
DATE 2-15-72	
DRAWING No. 365A-S1	REV. ECO 634 9-6-72

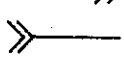
Technical Information

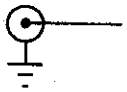
STANDARD DRAFTING SYMBOLS, ELECTRONIC


Connection to any given voltage.

Line ending at the edge of the sheet indicates continuance on another sheet.


Male pin or card edge contact.


Female pin, socket or card edge connector.


Coaxial connector.


No connection.

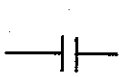

Connection.

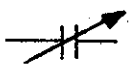

Resistor, 1/4 W, ±5% value in ohms (unless specified otherwise).

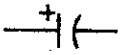
Resistor, 1/4W, ±1%, value in ohms (unless specified otherwise).

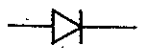

Resistor, variable, any type.

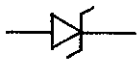

Resistor, variable, any type.

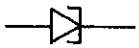

Capacitor, ceramic disc. Value in microfarads (unless specified otherwise).


Capacitor, variable. Values in Picofarads (unless specified otherwise).


Capacitor, polarized. Values in microfarads/volts (unless specified otherwise).

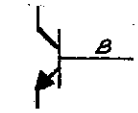

Diode, signal or rectifier.


Diode, zener.

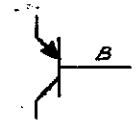

Diode, tunnel.


Diode, snap.

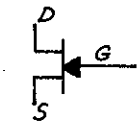

Light emitting diode (LED).



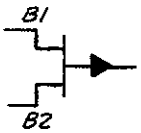
NPN Transistor.



PNP Transistor.



Field effect transistor, P Channel.



Field effect transistor, N.


Air choke.


Ferrite bead.


Ferrite core choke, Z 500 ohms when f ≥ 60 MHz (unless otherwise indicated).


Ferrite core choke, 40 uH, (unless otherwise indicated).

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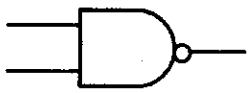
STANDARD DRAFTING SYMBOLS, INTEGRATED CIRCUITS.
TRANSISTOR - TRANSISTOR LOGIC (TTL).

The drafting symbols used are patterned after MIL STD 806, with some modifications. Shown below are some of the more commonly used symbols. Letter designations in the IC symbols correspond to those on the printed circuit layout. (In the case of multi-channel circuits, the designation will normally consist of two letters, the first one being channel identification.) Pin connections are identified by the number located on input and output lines. (For outline drawing, see next page).

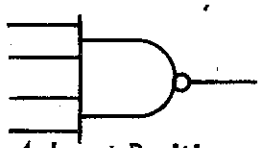
Positive logic notation is used. Logical "0" is nominally zero Volts and logical "1" is nominally 2.5 Volts.

Supply voltages of IC's are shown in a table on each schematic.

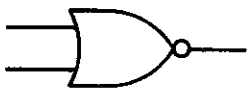


2-Input Positive NAND Gate

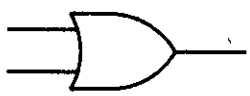
2-Input Positive AND Gate



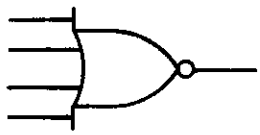
4-Input Positive NAND Gate



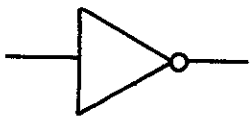
2- Input Positive NOR Gate



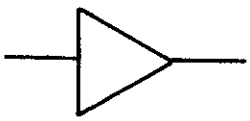
2 -Input Positive OR Gate



4-Input Positive NOR Gate



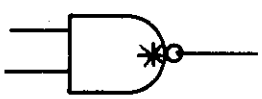
Inverter or Inverting Buffer



Non-Inverting Buffer

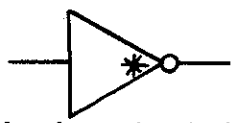
Exclusive OR Gate

Open collector outputs are identified by an asterisk (*) on the output connection.



2-Input Positive NAND Gate W/Open Collector

2-Input Positive OR Gate W/Open Collector



Non Inverting Buffer W/Open Collector

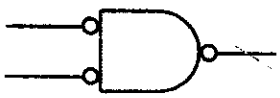
Technical Information

STANDARD DRAFTING SYMBOLS, INTEGRATED CIRCUITS
EMITTER - COUPLED LOGIC (ECL)

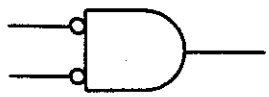
The drafting symbols used are patterned after MIL STD 806, with some modifications. Shown below are some of the more commonly used symbols. Letter designations in the IC symbols correspond to those on the printed circuit layout. (In the case of multi-channel circuits, the designation will normally consist of two letters, the first one being channel identification.) Pin connections are identified by the number located on input and output lines. (For outline drawing, see next page).

Logical "0" is nominally -0.8 Volts and logical "1" is nominally -1.6 Volts.

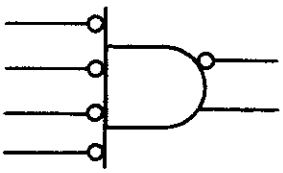
Supply voltages of IC's are shown in a table on each schematic.



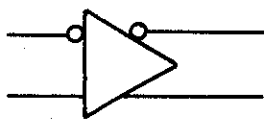
2 - Input Gate.
Negative AND (Positive OR) Gate.



2 - Input Gate.
Negative NAND (Positive NOR) Gate.

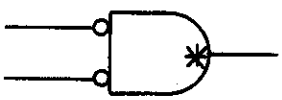


4 - Input Gate.
Negative AND/NAND (Positive OR/NOR) Gate.

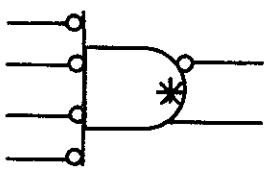


Differential
Amplifier.

Open emitter outputs are identified by an asterisk (*) on the output connection.



2 - Input Negative NAND Gate.
With Open Emitter.

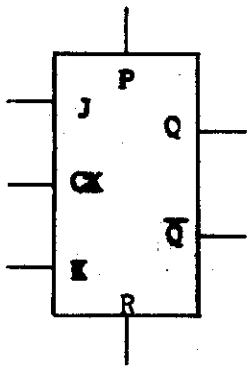


A - Input Gate.
Negative AND/NAND (Positive
OR/NOR) Gate.

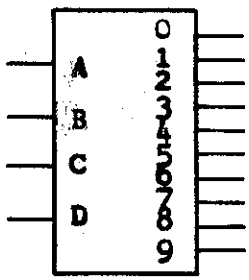
Technical Information

STANDARD DRAFTING SYMBOLS, INTEGRATED CIRCUITS.
TRANSISTOR - TRANSISTOR LOGIC (TTL) OR
EMITTER COUPLED LOGIC (ECL).

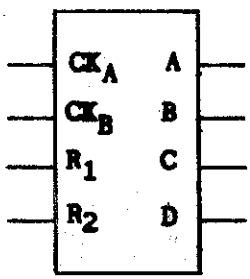
Flip-Flops and other MSI integrated circuits are generally drawn as a rectangular box with connections marked inside the outline. Some abbreviations are: R - Reset (or Clear), P - Preset (or Set), CK or CLK - Clock, etc. Some typical examples are shown below. See the manufacturer's specification for additional information.



J-K Master-Slave
Flip-Flop

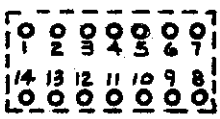


BCD-To-Decimal
Decoder-Driver



Binary Counter

Orientation of pin numbers of any DIP (Dual-In-Line-Package) is shown below. Pin 1 will normally be identified on the printed circuit board.



Bottom View

ENGINEERING DEPARTMENT
LeCroy Research Systems Corp.