First Evaluation of Neutron Induced Single Event Effects on the CMS Barrel Muon Electronics.

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Abstract

Neutron irradiation tests of the available electronics for the CMS barrel muon detector were performed using thermal and fast neutrons. The Single Event Upset rate on the Static RAM was measured, while upper limits are derived for devices having experienced no failure. The results are used to guess the the mean time between failures in the whole barrel muon detector.

I. INTRODUCTION

The LHC detectors will be working inside the highest radiation field ever experienced in high energy physics. Several studies were done in order to check the radiation tolerance of the detector itself and investigations were done in order to assess the tolerance of electronics.

The barrel muon chambers are a particular case within the general scenario. The radiation dose absorbed after ten years of operation at LHC is negligible (less than 0.2Gy). The expected neutron fluence is not high enough to generate a relevant bulk damage (less than 2.5×10^{10} n/cm^2), nevertheless detector electronics could still be disturbed or even damaged because of Single Event Effects (SEE). Besides it will not be accessible, since most of it is located within the cavern, lodged on the chambers.

We expect therefore that most of the reliability of these electronics will be associated to the probability of occurrence of these rare Single Event Effects induced by the interaction of the ionizing particles with the silicon.

II. NEUTRON BACKGROUND EXPECTATIONS

Muon chambers are shielded by the iron yoke against the effects of charged low energy particles, and the background particle flux will be dominated by neutrons thermalizing within the cavern. Neutrons are produced all around inside the cavern by beam halo interactions with magnets on the LHC beam line and the detector itself.

Extensive simulation studies [1] were done to estimate the rate of background particles at all positions inside CMS. The results of the simulation are shown in Figure 1, where the energy spectra of neutrons at different positions in the detector are reported. Although the Montecarlo calculations for low energy neutrons are usually affected by large errors, we have an indication of the expected neutron rate. We see that the neutron background is linearly decreasing with energy and is naturally ending around 100 MeV in the outermost station and at few hundred MeV in the innermost one, that is suffering from high energy neutrons flooding through the CMS calorimeters and coil. The fast and thermal neutron fluence are expected to be each one around 500 n cm^{-2}s^{-1}.

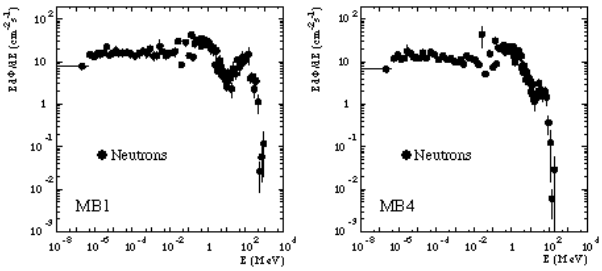

Figure 1: Expected neutron fluence through the innermost (MB1) and the outermost (MB4) muon barrel stations.

III. SINGLE EVENT EFFECTS PHENOMENOLOGY

The Single Event Effects are associated to individual ionizing particles and their occurrence is given as a cross section that provides the probability that a neutron hitting a squared centimetre of a silicon device produces a SEE.

The most likely common effect is called Single Event Upset (SEU) and affects all kinds of memory devices (SRAM, DRAM and FLASH memories, microprocessors and DSPs, FPGAs and logic programmable state machines, etc.). It is detected as a modification of the memory state and is usually recoverable by data rewriting. Memory upset is caused by the deposition, inside a device sensitive node, of a charge higher than a given threshold. This charge value is dependent on both technology and device layout [2]. Even system architecture plays a relevant role in SEU sensitivity: critical data can be protected either using less sensitive technologies or implementing redundant logic. Occasionally the energy deposition associated to the interacting particle can be the cause of a latch-up (SEL) or a gate rupture (SEGR) or even a device burnout (SEBO) [3]: these effects could be destructive and generally cannot be recovered. Both SEL and SEBO

effects can be reduced by system architecture design. As a matter of fact, while the permanent damage associated to SEL can be eliminated using power supply and input-output overcurrent protection circuitry, the power device burnout probability can be reduced to a safety level limiting the operating voltage to a fraction of the breakdown value.

All the measurements done until now confirm that the SEU probability is depending both on the technology used for integrated circuits production and on the processing chain actually used in the factory. The associated technological parameters are usually not well controlled since two orders of magnitude in the quoted results are a typical variation.

Very recent tests [4] proved that thermal neutrons are causing SEU. The responsible mechanism could be neutron capture from the ^{10}B isotope (19.9% of natural boron), normally present in semiconductor technologies as a result of doping and in the glass passivation layer, followed by nucleus de-excitation with α-particle emission through the reaction $^{10}B(n,\alpha)^{7}Li$. Both the lithium nucleus and the α-particle release locally enough energy to cause the memory cell change of state [5,6].

Fast neutrons interact with ^{28}Si atoms producing relevant recoil energy already at neutron energy around 0.1 MeV,but only neutrons with an incident energy higher than 3 MeV should contribute to the SEU cross section: the relevant reactions are in fact $^{28}Si(n,p)^{28}Al$ with a 4 MeV threshold and $^{28}Si(n,\alpha)^{25}Mg$ with a 2.7 MeV threshold [5]. Published results claim that SEU cross section has an energy threshold and is slowly increasing with energy up to a saturation value at 100 MeV neutrons energy [6].

In this scenario, the whole existing literature agrees that, if the neutron background is going to be a problem, the existing data cannot be used directly to estimate SEU probability of a device, unless you can tolerate large safety margins. It is therefore recommended to get oneself own measurements done .

IV. MEASUREMENTS SETUP

CMS barrel muon detector electronics will deal with a wide spectrum of neutron energies. Our irradiation tests aim to evaluate effects due to the fast neutrons below 100 MeV or the thermal portion of the neutron spectrum.

Low energy neutrons are copiously produced in the nuclear laboratories by scattering of proton or deuteron nuclei accelerators on low atomic mass nuclei targets.

The Van de Graaff accelerator at INFN laboratory of Legnaro (LNL) produces neutrons through the reaction $^{9}Be(d,n)^{10}B$, with a maximum deuteron energy of 7 MeV. The neutron rate is high enough to allow an easy integration of ten LHC years in a short time. The emitted neutron spectrum [7] is shown in Figure 2a for several incident deuteron energies. The emitted neutron spectra high-end is limited to about E_n = 11MeV.

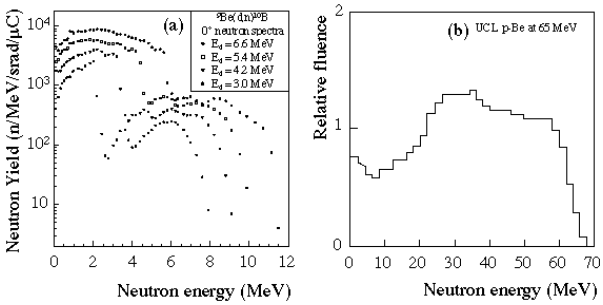

Figure 2: Neutron fluence (a) at LNL and (b) at UCL

The UCL laboratory provides a facility for a wide neutron spectrum using the reaction $^{9}Be(p,n)^{9}B$, with a maximum incident proton energy of 65 MeV optionally cleaning the neutrons with a polyethylene/iron filter. The spectrum in our test setup is shown in Figure 2b: the neutron energy is roughly flat in the range 20-60 MeV.

Thermal neutrons were generated at LNL using the first reaction. The moderator [8] is sketched in Figure 3. The Beryllium target is enclosed in an heavy water tank surrounded by very thick graphite walls. The fast neutrons produced in the d-Be scattering are therefore moderated by the heavy water and reflected from the graphite, thermalizing and remaining inside the graphite. The irradiation cavity is situated on top of the heavy water tank in backward position with respect to the beryllium target in order to minimize the residual fast neutron content.

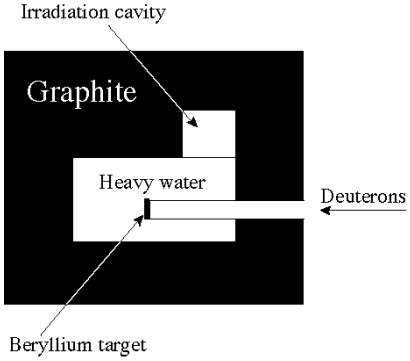

Figure 3: Sketch of the neutron moderator.

The devices ready to be tested were the first prototype of the slow control board, the readout front-end board and a prototype trigger board. The list of relevant integrated circuits is shown in Table 1: in particular three control boards were tested.

Device registers were initialized to a standard pattern, verified by the readout system with a two seconds cycle. Every time an alteration of the memory state was detected, the time, the integrated current on the target, the address and the datum were stored for data analysis.

Table 1: List of tested components with relevant characteristics of each device.

Device	Productor/Type/Year
Low Drop Regulator	MICREL/29501-3.3BU/1997
µP	MOTOROLA/MC68HC16/1994
FLASH	ATMEL/AT29C101A-12PC/1996
SRAM	SONY/CXK581000AM-70LL/1993
EPROM	ATMEL/AT27C512R-15JC/1995
Optical transceiver	HONEYWELL/HFM2600-1 /1998
ASIC TSS	ES2 0.7 µm / TOP5 ceramic package/1997
ASIC BTI	ATMEL 0.5 µm/LTCC substrate & in dies /1997
ASIC MAD	AMS 0.8 µm/BiCMOS/1997

V. SEU CROSS SECTION EVALUATION

The test aimed to the observation of Single Event Upsets due to thermal or fast neutrons and to the determination of the cross section for every device. The existence of thresholds and its dependence on neutron energy was investigated as well as the uniformity of behaviour among different pieces of the same device.

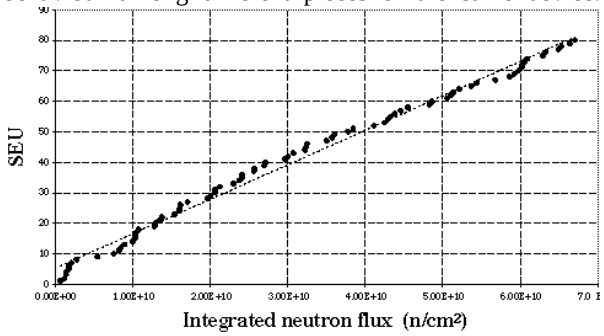

Figure 4: SEU progressive number versus integrated neutron flux in the thermal neutron run.

A. Thermal neutrons

The boards were irradiated with thermal neutrons on four data taking periods. Since the neutron flux inside the graphite is modified by the inserted boards, we had to get the actual neutron flux measuring the activation of Indium and Cadmium-Indium (to get non thermal contribution) targets placed just in front of the integrated circuits.

After a total rate of ~$7x10^{10}$ n/cm^2 the only device experiencing SEU was one of the SRAMs. Figure 4 shows the plot of the SEU numbers versus the integrated neutron dose for all the test periods. The fact that the results are sitting on a line is an indication that there are no total dose effects, i.e. no saturation due to device degradation. The slope of the average line fitted in this plot is a measurement of the SEU cross section of the device. Results are collected and summarized in Table 3.

B. Threshold search

As we already stressed there is some evidence that an energy threshold on fast neutrons induced SEU probability is existing. The known processes indicates that this threshold should be in the few MeV region. As evidenced by the momentum spectra of Figure 2a, the neutrons produced in the $^9Be(d,n)^{10}B$ reaction were not monochromatic. Measurements with the thick Beryllium targets using different incident deuteron energy are nonetheless useful to give an indication of the existence of a threshold, since the fraction of neutrons with E_n > 1MeV in the production spectra is largely modified as a function of the beam energy.

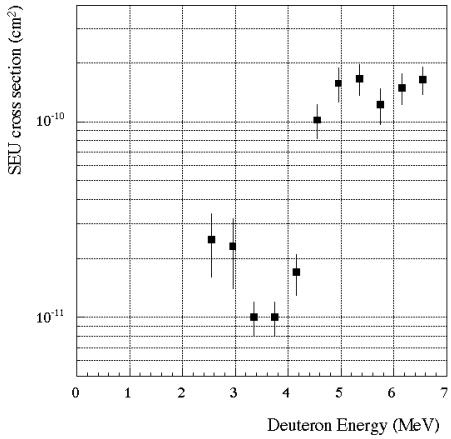

Figure 5: Rough SEU cross section evaluation on SRAM # 1as a function of the incident deuteron energy.

The SEU cross section as a function of the incident deuteron energy evaluated considering an equal contribution from all neutrons produced is shown in Figure 5. Its behaviour is consistent with the existence of a threshold around 3 MeV, as loosely determined folding this distribution with the spectra of Figure 2a. This result agrees with the opening thresholds of the $^{28}Si(n,p)^{28}Al$ and $^{28}Si(n,\alpha)^{25}Mg$ reactions in addition to the neutron elastic scattering on silicon.

Table 2: Comparison of SEU probability for SRAMs of same type and lot on different test conditions explained in the text. Errors (about 50%) are not included for sake of clarity.

	SEU probability (cm^2) on SRAM					
	#1	#2	#3	#4	#5	#6
Thermal	$1.13x10^{-09}$	$<1.38x10^{-10}$				
LNL	$7.03x10^{-10}$	$4.28x10^{-12}$	$6.28x10^{-11}$	$4.41x10^{-12}$		
UCL	$1.03x10^{-08}$	$8.99x10^{-11}$			$1.50x10^{-10}$	$1.70x10^{-10}$

C. Fast neutrons at E_n < 11 MeV

A complete test was done only at E_d = 6.5 Mev integrating a total rate of ~10^{12} n/cm^2 .

We used the MCNP Montecarlo code to determine the neutrons flux expected through our devices with a careful description of the setup area in order to account for neutrons scattering on the walls, the floor and on the relevant devices inside the measurement area.

As expected after the thermal neutron test, we had a large number of SEU from SRAM#1. The SEU number at Ed = 6.5MeV is shown as a function of time in Figure 6.

With fast neutrons we could observe also SEU on SRAM#2. Although this RAM is of the same type and production lot, we obtained a SEU cross section two orders of magnitude lower than SRAM#1 (4 SEU after 1.52x10^{12} n/cm^2 against 135 SEU after 0.75x10^{12} n/cm^2). Thus we experienced the effect reported in the existing literature of big variations for the same device.

Results are collected in Table 2 assuming that only neutrons with E_n > 3 MeV contribute to the cross section.

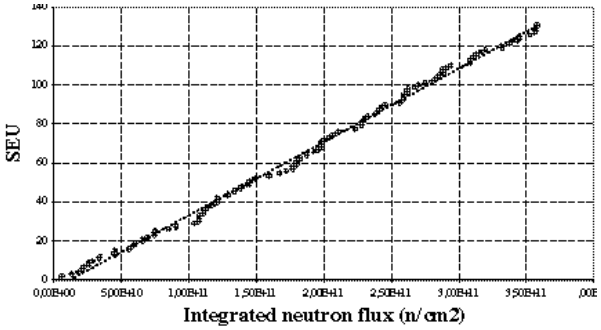

Figure 6: SEU progressive number on SRAM # 1 versus integrated neutron flux at E_d = 6.5 MeV

D. Fast neutrons at 10 < E_n < 70 MeV

Another effect reported in literature is the dependence of SEU probability on neutron energy. The data taken during the LNL test were limited to energies barely exceeding the threshold and one order of magnitude lower than the expected maximum neutron energy at LHC. We completed this preliminary investigation testing the devices at UCL using a 65 MeV proton beam incident on a beryllium target. The integrated neutron flux was again ~10^{12} n/cm^2. Globally we tested 6 SRAM of the same type and lots: results are compared in Table 2.

Looking at the table we see that we have variation up to two orders of magnitude for the SEU probability of the SEU probability depending on the piece we irradiated. Instead considering the same piece we found an increase of the probability of a factor ~20 with deuteron energy and therefore a clear important dependence on neutron energy.

While none of the other devices underwent SEU on the lowest energy run, at UCL we registered some of them on the 1 kbyte microprocessor internal RAM. The probabilities were 3.85x10^{11} cm^2 and 1.25x10^{11} cm^2 for the two tested pieces. Comparing the fault probability per bit of the SRAM and the microprocessor (128 kbytes versus 1 kbyte) we find that the latter is of the same order of the worst RAM (~10^{-15} cm2/bit).

E. SEU uniformity verification

It is interesting to check if there are more sensitive positions inside the SRAM, or if the probability of a SEU happening inside the chip is equally distributed.

We verified that the address was not always the same and that also the bit of the data word changed was not repeating finding: no preferred bit flipping within the statistics precision.

Another interesting check is the verification if the bit change from High → Low was more probable than the one from Low → High. Figure 7, taken from a thermal neutron run, supports the understanding of an homogeneity of the SEU cross section.

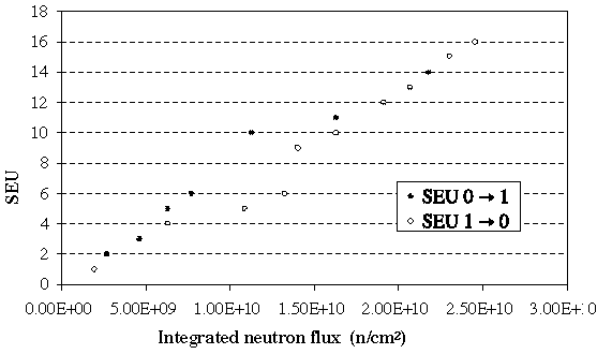

Figure 7: SEU on SRAM # 1 by type of bit modification

VI. SEE ON MUON FRONT-END

The readout front-end electronics is composed by a charge integrator and a variable threshold discriminator. Since the front-end circuit is a charge sensitive device, the SEE associated to it is the detection of energy deposition inside the circuit simulating a pulse over threshold.

Two prototypes were tested both on thermal and fast neutrons. Since access to the boards was easy we modified the threshold settings in order to verify that SEE cross section was depending on the actual threshold.

Figure 8 reports the SEE cross section in the threshold scan run for fast neutrons. In this case the quoted SEE cross section assumes that all neutrons in the spectrum have the same probability to induce a SEE. The systematic errors cannot be estimated, but the result is well below the input noise expected from interactions inside the gas volume. Hence we can state that we don't expect problems with noise induced from SEE on the front end readout electronics.

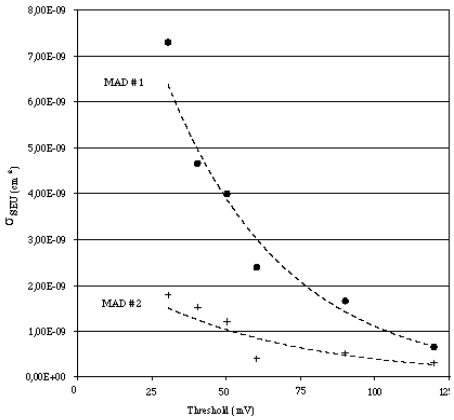

Figure 8: SEE on front end device as a function of discriminator threshold at E_d = 6.5 MeV.

VII. CONTROL SYSTEM BLOCKS

We had some system blocks associated to corruption of the program inside the RAM that were solved by automatic program reload. But in some cases we were forced to give an external hardware reset. While this problem occurred only once at low energy it was much more frequent at high energy: the estimated cross section of this major problem is $(2.5\pm0.5)\times10^{-11}$ cm^2.

VIII. RESULTS SUMMARY

Results of the various tests are collected in Table 3 considering only the worst result for each device. We quote a 90% confidence level upper limit of the SEU cross section for all the integrated circuits which experienced no failure. The error in the SRAM SEU cross section is the squared sum of statistical and systematical error. The latter one is due to the uncertainty of the total neutron flux and is dominating our calculation. The Mean Time Between Failures is computed for the whole barrel muon detector, considering the number of pieces of each chip used in the electronics layout. We considered 50000 BTI chips and few hundred pieces of the other devices.

IX. RADIATION DAMAGE VERIFICATION

After the whole bunch of tests, each device was irradiated with more than 2×10^{12} n/cm^2, equivalent to the expected flux after more than twenty years of operation at LHC. We therefore verified the status of each device after irradiation to see if the neutrons had produced any permanent damage. The only device showing a deterioration was the Trigger Server ASIC (TSS), which was drawing a standby current increased by 10% with respect to the same current as measured before the tests. Besides none of the devices underwent a destructive SEE.

X. CONCLUSIONS

We measured neutron induced SEE both in the fast energy region below 70 MeV and in the thermal energy region and gave a first measurement of SEU cross section or derived upper limits for some devices to be used in the muon barrel electronics. Some evidence of a threshold and energy dependence of the cross section was found.

XI. REFERENCES

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Table 3: SEU cross section and expected mean time between failures in the whole CMS muon barrel detector due to neutrons of different energy. We considered 500 n/cm^2 of thermal neutrons, 20 n/cm^2 with $3<E_n<10$ MeV and 30 n/cm^2 with $E_n>10$ MeV.

	SEU cross section (cm^2)			Mean Time Between Failures (hours)		
Device	Thermal	LNL	UCL	Thermal	LNL	UCL
LD reg	$< 1.38\times10^{-10}$	$< 1.40\times10^{-11}$	$< 1.00\times10^{-12}$	< 64	< 15587	< 147892
µP	$< 1.38\times10^{-10}$	$< 1.40\times10^{-11}$	3.85×10^{-11}	< 385	< 95340	23088
FLASH	$< 1.38\times10^{-10}$	$< 1.46\times10^{-12}$	$< 1.00\times10^{-12}$	< 385	< 91101	< 474734
SRAM	$(1.13\pm0.2)\times10^{-9}$	$(7.03\pm0.2)\times10^{-10}$	$(1.03\pm0.2)\times10^{-8}$	23.5	1263	23
EPROM	$< 1.38\times10^{-10}$	$< 1.61\times10^{-11}$	$< 1.00\times10^{-12}$	< 385	< 83043	< 474734
Optolink	$< 1.38\times10^{-10}$	$< 1.43\times10^{-11}$	$< 1.00\times10^{-12}$	< 385	< 93231	< 474734
ASIC TSS	$< 2.68\times10^{-10}$	$< 9.46\times10^{-12}$		< 33	< 32225	
ASIC BTI	$< 1.75\times10^{-10}$	$< 1.31\times10^{-11}$	$< 1.00\times10^{-12}$	< 1.5	< 507	< 4436