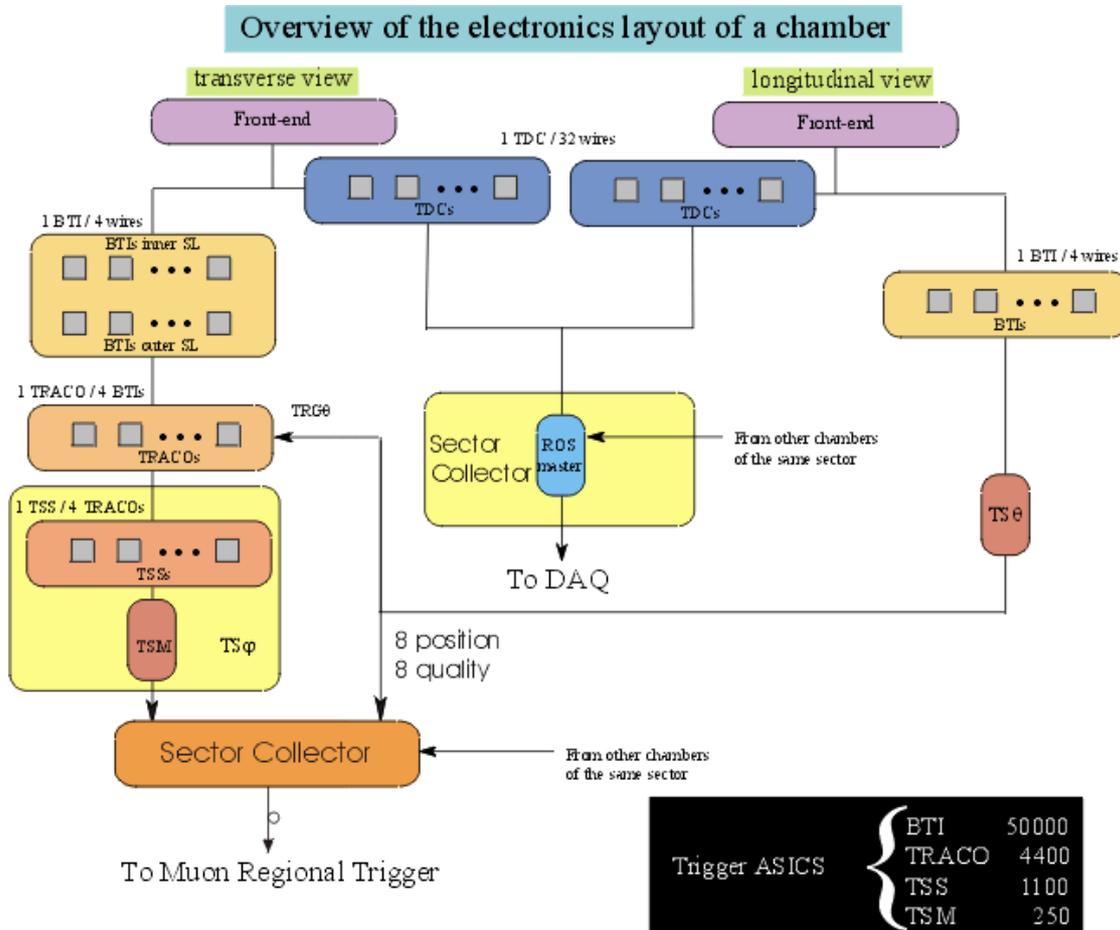


9.3 System Overview

The block scheme of the primitive generator for the first level trigger is shown



in Figure 9.03.01.

Figure 9.03.01: Overview of DTBX on-board electronics.

In both transverse and longitudinal views the front-end trigger device, called Bunch and Track Identifier (BTI), is performing a rough track reconstruction with identification of the parent bunch crossing. The BTI output, delivered at constant latency, consist of angle and position of the candidate track accompanied by a quality bit to identify tracks with good hits in all the four tube plains of the Superlayer.

In the longitudinal view BTIs are programmed to trigger only on tracks pointing to the vertex. Trigger strobes and quality bits are summed at different levels to reduce the spatial resolution by a factor 8. The 8 trigger bits and the 8 quality bits are used like an odoscope with a resolution of 32cm and are delivered to the theta view Track Finder.

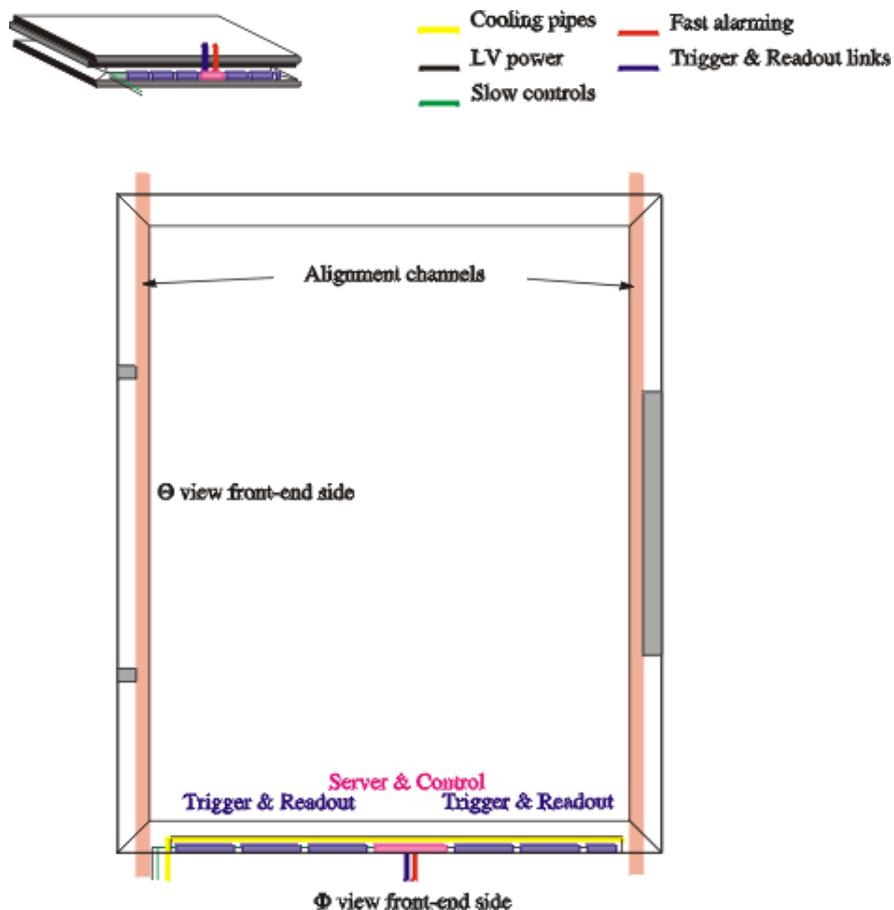
In the transverse view, BTI output data (angle, position and quality of the crossing track) are sent to the Track Correlator (TRACO), the next stage in the trigger chain. This device is required to associate two track segments of the transverse view among them, enhancing angular and position resolutions. Since each TRACO is connected to many BTIs, track sorting is needed to limit the amount of output

information. TRACO delivers angle, position and quality of the two best candidate tracks chosen looking for the lowest bending angle.

Each chamber is equipped, depending on its dimension, with a variable number of TRACOs, from 12 to 25. In order to reduce the amount of chamber trigger information, a third stage in the chamber trigger chain was necessary, performing track sorting and candidate selection. This task is accomplished by two ASICs. First the Track Sorter Slave (TSS), performs data reduction selecting the two best candidate tracks among the possible eight delivered by four TRACOs. Three to seven TSS are connected to the Trigger Sorter (TS) that is performing a further data reduction to a maximum of two candidate tracks per chamber per bunch crossing. Other important functions are embedded in TRACO, TSS and TS: noise filters, coordinate conversion, self-test and emulation.

The trigger information in the transverse view consists of two track segments with bending angle, position and quality while, in the longitudinal view, it consists of 8 bits giving the position of all the crossing tracks pointing to the vertex accompanied by 8 quality bits. Trigger data are sent to the Sector Collector unit via copper cables using LVDS signals. In this unit, lodged in the fourth station chamber, are grouped all trigger and readout optical links for data transmission to the Regional Trigger and to the DAQ.

Chamber trigger and readout electronics is lodged in Mini-Crates (MC) mounted on the front side of the chamber, inside the C profile surrounding the



honeycomb layer (Figure 9.03.02).

Figure 9.03.02: DTBX first station Mini-Crate location.

Low and high voltage power supplies are lodged on the balconies in crates powering half a wheel each. MCs trigger and readout data in each sector are sent to the Sector Collector (SC) unit that is integrated in the fourth station mini-crate. Chamber trigger and readout electronics is arranged in 128 channel units; only for the first and the fourth stations a 32 channel unit is necessary for a better matching with chamber channel number. A pictorial view of first station mini-crate without front panels is given in Figure 9.03.03.

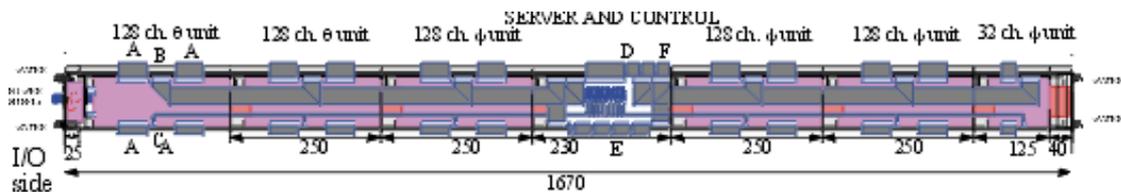
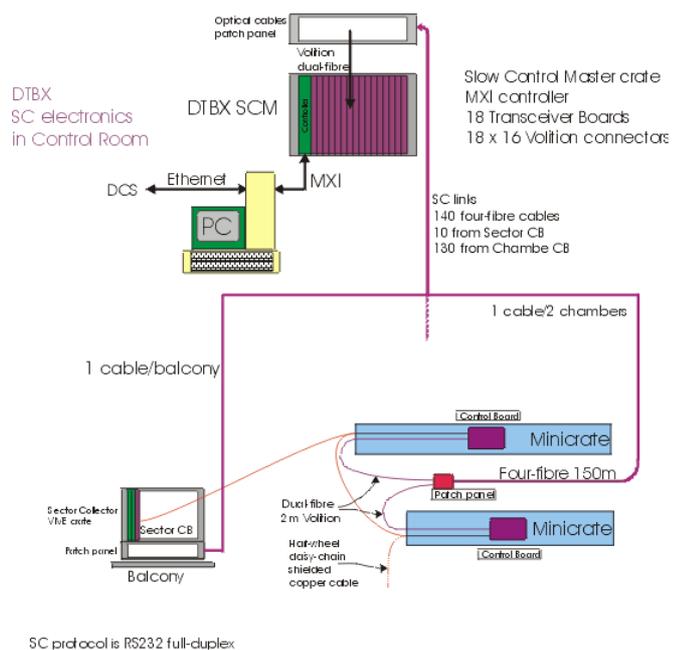


Figure 9.03.03: Pictorial view of DTBX first station Mini-Crate without front panels.

Inside the MC a Chamber Control Board (CCB) takes care of electronics setup, monitoring and of many control and test functions. One TTC receiver chip is lodged on the CCB for clock and broadcast signals distribution. Each CCB is connected via a dedicated optical fiber to the Master Slow Control (MSC) crate in Counting Room. As back-up channel a copper cable connects in parallel all MCs belonging to each half wheel to a Balcony Control Board (BCB) sitting on the balconies. Each BCB is connected to the MSC via dedicated optical fibers. MCs are connected to front-ends of both phi and theta Superlayers and to alignment and RPC electronics for remote controls via two dedicated I2C buses. MCs are cooled by cold water flowing in tubes extruded in the MC aluminum profile for the full length.

9.3.1 Slow Control Interface

The Master Slow Control, directly interfaced to the Detector Control System, interacts with each CB via a dedicated optical asynchronous serial bus called SC1 (Figure 9.03.04). A fiber pair is needed per chamber to communicate with the Control Board. For budget reasons SC1 lines are grouped in cables of four fibers. Patch panels are foreseen both at the barrel, near drift chambers and at the Master Slow Control crate in Counting Room. Patch panels consist of small boxes that, for the chamber side, are mounted on the iron between stations 1 and 2 and between station 3 and 4 to service the



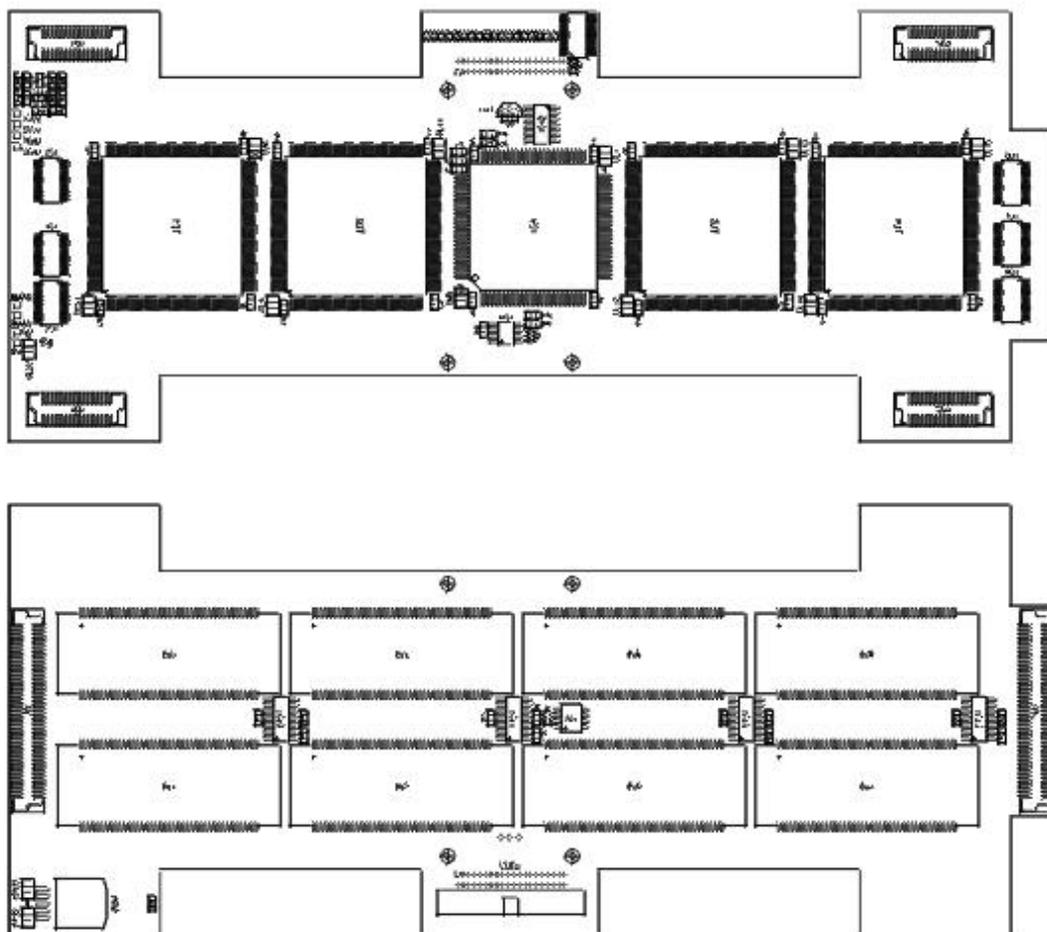
respective chambers.

Figure 9.03.04: Layout of DTBX Slow Control System.

An additional RS-485 connection, called SC2 is foreseen as slow control backup in case of failure of the optical one. The SC2 line connects in parallel all chambers in each half wheel and is serviced by a Wheel Control Board sitting on the balconies. The ten WCBs are connected with dedicated optical fibers to the Master Slow Control crate consisting of 17 Receiver Boards interfaced to a host PC via MXI bus. The connection between the Master Slow Control and the Detector Control System is via ethernet interface.

9.3.2 Trigger Boards

Trigger electronics is grouped in 128-channel units. An additional 32-channel unit is needed in the first and fourth stations to match the channel number. There are three types of different boards: two for the phi view, a 128-channel one called PHITRB128 and a 32-channel one called PHITRB32. PHITRB128 contains 32 BTIs assembled in 8 multi-chip modules (BTIM) connected to 4 TRACOs and one TSS (Figure 9.03.05), while PHITRB32 contains 2 BTIMs, one TRACO and one TSS (Figure 9.03.06).



For the theta view only a 128-channel unit exist called THETATRIB containing 32 BTIs assembled on 8 BTIMs (Figure 9.03.07).

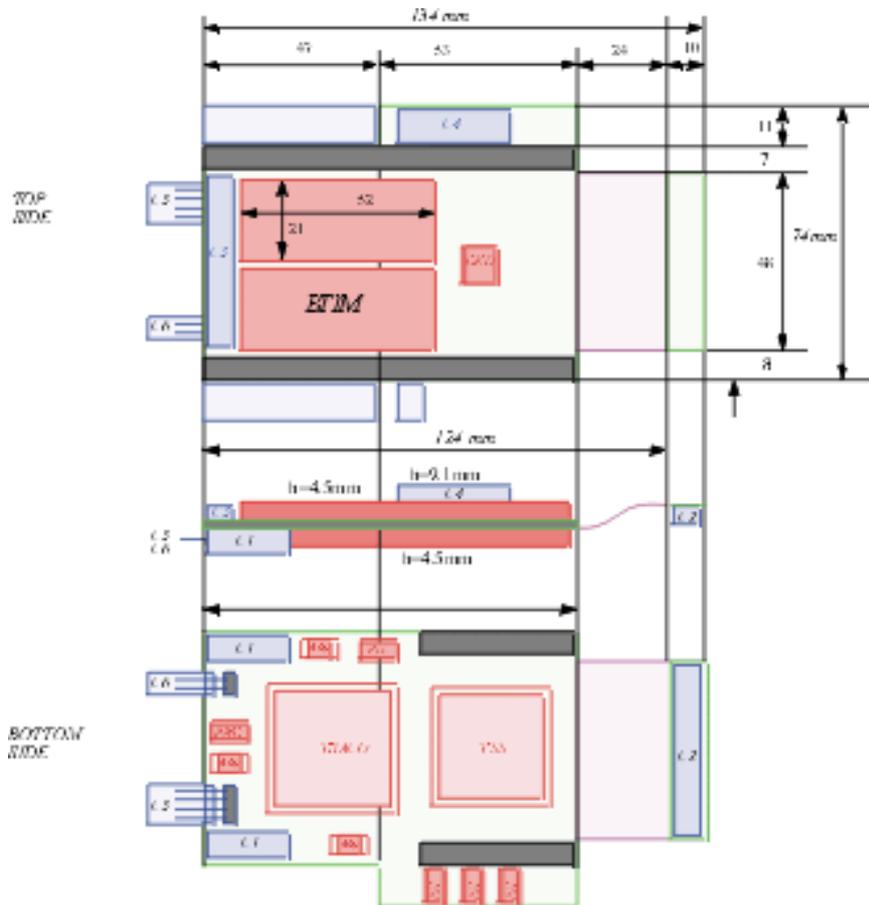


Figure 9.03.06: Sketch of PHITRB32 layout, the 32 channels board for DTBX transverse plane trigger

Front-end signals are received through the faced Readout Board, where LVDS to CMOS translators are located, while trigger data are sent to the Trigger Server via a fine-pitch 40 lines flat cable. Fine pitch lateral connectors are used for neighboring unit communications of detector signals and of chamber control signals coming from the central Server and Control unit.

Trigger Board power supply is internally stabilized to 3.3V by a low drop regulator. The external power supply, distributed via the mini-crate bus-bar, must be higher than 3.8V, at MC input, to guarantee operating conditions. The internal regulator has power supply protection circuitry with over and under voltage tolerance up to $\pm 40V$ and overcurrent limit with a “retriggerable fuse” function useful for latch-up protection. In case of power supply overload the internal regulator shuts off for a fixed amount of time allowing the power line voltage to go to zero and then turns on trying to restore automatically. In case of a persistent overload the sequence is repeated cyclically unless the Control Board, detecting the power failure, shuts off the regulator definitively.

Each Trigger Board can be shut off independently thanks to an “intelligent” on board regulator and input signal isolation logic. Local power supply measurement and control is accomplished by the Control Board that takes care of device turn-on and turn-off sequences.

Clock is distributed using PECL signals on twisted pair cables. One clock input with low skew is foreseen per Trigger Board. A low-skew clock distribution tree, consisting of PLLs and multiple drivers, is implemented in each TB. First the 40MHz PECL input clock is translated to CMOS by a receiver chip. A double PLL unit is used to generate the internal clocks at 40MHz and 80MHz, as needed by trigger ASICs. Buffers are used to provide a total of 37 clock lines at 40MHz and 32 at 80MHz. The maximum allowed skew from TTC output to ASIC input is about 1ns.

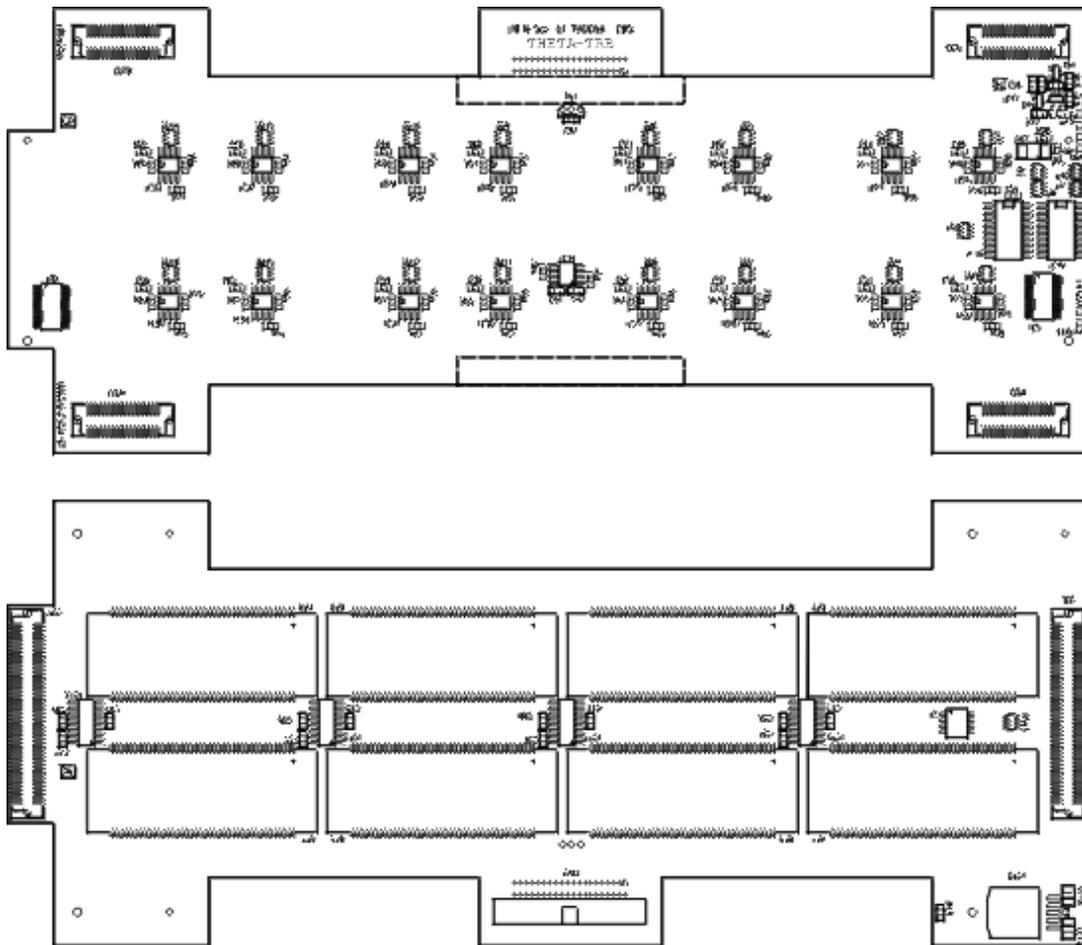


Figure 9.03.07: Layout of THETA-TRB, the 128 channels board for DTBX longitudinal plane trigger.

Trigger Boards can be tested at many levels using a JTAG bus and on-board self-test features. The Control Board can address a single Trigger Board for JTAG access, up to a maximum of 16 units, in order to reduce the component chain. A production assembly test is foreseen using boundary scan and on-board functional tests using event emulation capabilities integrated in BTI test logic. Once the Trigger board is programmed in Test Mode, emulation data, consisting of the delays in 12.5ns steps of event hits, are downloaded to all BTIs via JTAG. A trigger command issued via JTAG and internally synchronized with the 40 MHz clock starts the test sequence. Trigger data can be latched at Trigger Board output or readout via JTAG, downloading the content of snap registers integrated in all ASICS. This kind of functional test can be repeated for assembled Mini-Crates allowing a full test of trigger functionality without any external test pattern generator.

9.3.3 Server Board

The Server Board (SB), one per Mini-Crate, takes care of Trigger Server functions. The Trigger Server Master consisting of three chips is lodged on it.

This unit is powered with three separated 3.3V lines, one per ASIC, in order to maintain the highest possible redundancy. Overcurrents, on power supply lines, are protected by precise current monitors with fast shut off capability.

Server Board clock phase is adjustable with respect to the Trigger Board clocks to take care of signals synchronization.

SB: Descrizione delle funzionalita' del TSM per viste phi e theta.

Figure 9.03.08: Server Board block scheme.

9.3.4 Control Board

The Control Board, as part of the Slow Control Unit accomplishes control and monitoring functions of mini-crate electronics; pictorial views of chamber Control Board and Server Board are shown in Figure 9.03.09 and 9.03.10.



Figure 9.03.09: Sketch of SCU layout, the Control Board of DTBX mini-crate electronics.

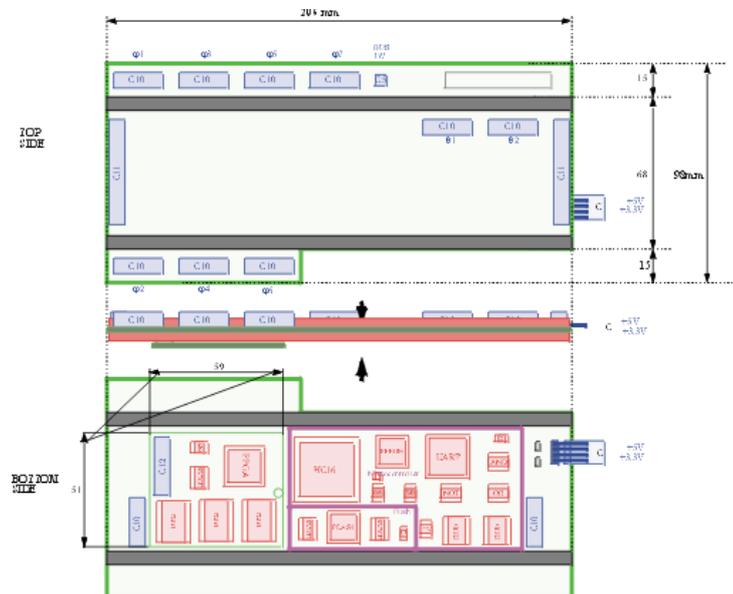


Figure 9.03.10: Sketch of SCU layout , the Server Board of DTBX mini-crate electronics.

An on board microprocessor has access, either via JTAG or via a parallel interface, to all ASIC configuration registers. The chamber TTC receiver, used as clock and broadcast commands source, is located on the CB. CB functionality can be grouped in different units: clock distribution, test pulse, front-end analog signals, slow control interfaces, temperature measurement, power supply distribution and microprocessor unit (μ PU).

Clock distribution logic consist of three blocks of PECL buffers delivering dedicated low skew clock lines for Trigger Boards, Readout Boards and Server Board. Each block can be independently enabled or disabled by the μ PU. Clock cables consist of twisted pairs cut precisely in order to guarantee the same sampling clock phase at BTI inputs for all the three Superlayers.

The Test Pulse unit is able to inject a fixed and repeatable amount of charge into front-end inputs at the reception of a defined command. Furthermore, programming the unit is possible to simulate a track normal to the Superlayer and crossing it at any position with $10\mu\text{m}$ resolution, allowing a precise characterization of TDC and BTI-TRACO performances. In order to reduce the amount of calibration data, charge injection is masked either at front-end output or at Readout Board input, limiting the number of hit channels to 4 per Trigger and Readout Boards. The arrangement in Even and Odd channels and the grouping of channels at Readout Board input are shown in Figure 9.03.08. As an example to simulate a track in cell T1 both Even and Odd front-end channels must be active while only group A of readout channels is enabled. To simulate a track in cell T2 Even channels and groups A and B are enabled. A sequencer has been implemented in the Test Pulse logic to scan automatically all cells: every time a Readout Sequence Advance command is received the test sequence moves by one step changing the tested cell by one position on. Trigger electronics has a test sequencer built in all ASICs. For tracks in cells T1 and T2 only the first BTI per Superlayer is enabled, while for T2 the second one is activated. The same applies for TRACOs and TSSs that are enabled one at a time. Every time a Trigger Sequence Advance command is received the test sequence moves by one step changing the tested device by one position on. The μ PU takes care of Test Pulse unit signal handling once dedicated commands are received via TTC. A Test Pulse command initiates the charge injection sequence, a Test Pulse Advance command is used to scan the test sequence (both TTC-user commands) and an initial Test Pulse Reset command (TTC-system command) performs sequence initialization. Track position is programmable via Slow Control and is intended to stay fixed in a test sequence.

Front-end chips, called Multiple Amplifier and Discriminator (MAD) integrate all channel analog processing functions: amplification, discrimination and signal cable driving. MAD chips add new possible features to front-end electronics: input channels can be singularly enabled at the shaper stage, also an integrated temperature probe can be used for monitoring purpose.

For front-end operation three settings are necessary: the threshold voltage, the output pulse-width and the power supply consumption. Output pulse width is set to find the best compromise between electronic noise, signal cable loading and multi-hit separation capability. Changing the power supply consumption front-end performances can be adapted to chamber needs. Programming of front-end operating parameters is done setting dedicated analog voltages. Pulse width is set in the range xx-xx with a voltage (V_{width}) within 0.2V-4V at 5mV steps with a gain of xxV/ns,

while power consumption is programmed in the range xx-xx with a voltage (V_{bias}) within 0.2V-4V at 5mV steps with a gain of xxV/mW. Charge threshold in the range xx-xxfC is set by an analog voltage (V_{trh}) in the range $V_{bias} \pm 0.45V$ at 1mV steps with a gain of xxmV/fC..

Front-end electronics monitoring performs temperature and power supply measurements. Two temperature channels are provided with maximum and medium temperatures measured in MAD chips by dedicated cells. Medium values of 5V and 2.5V power supplies are measurable by other two channels. Front-end setting and monitoring of all analog voltages are separate for the three Superlayers with the exception of V_{width} : a total number of $3 \times 2 + 1$ analog voltages are generated and a total number of 3×4 analog voltages are measured by DAC and ADC Control Board circuitry. All generated voltages are read-back via dedicated ADC channels with 4.5mV resolution.

Temperature either in Readout and Trigger electronics or outside chamber mini-crate is measured using dedicated chips (DS1820 from Dallas Semiconductor) with single wire interface. For external temperature measurements a large number of chips can be connected to the Control Board temperature connector for a maximum of 300m cable length.

Control Board access is guaranteed by means of three serial interfaces, one intended for test purposes (called SCI) only and two for the detector Slow Control, as main (called SC1) and back-up (called SC2) accesses. The SCI is a standard RS-232 link that can be used in alternative to SC2, an RS-485 standard link, both running at 9600 baud. The SC1 is an asynchronous serial communication interface with optical connection for full duplex communication between the Master Slow Control (MSC) crate, sitting in Counting Room and chamber mini-crate electronics. While SC1 link is dedicated to one chamber, SC2 link is shared among all mini-crates of half a wheel.

Three I2C busses are provided dedicated to front-end, RPC and alignment electronics programming.

The Front-End Board (FEB) uses a Philips PCF8577 to control such features via an I2C bus interface. Through this chip 32 logical lines can be programmed: 16 are used for masks and other 4 for temperature control. 3 address lines can select a maximum of 8 devices sharing the same bus. Since a SL houses more than 8 FEB further addressing is required: a remote 8-bit bus expander, the Philips PCF8574, is used to select 6 groups of 4 FEBs allowing a total address space of 24 boards.

RPC I2C ...

Alignment I2C...

Readout and Trigger ASICs are programmed via JTAG. As already mentioned every Trigger and Readout Board has a JTAG chain useful for unit setting and testing. Boards can be accessed one at a time by means of chain addressing. Four lines are used to address a maximum number of 16 units. During normal operation mini-crate ASICs can be accessed for monitoring purposes without any interference with trigger and readout activity. To guarantee the capability to configure all trigger devices a back-up channel has been provided for device programming. Using the trigger data path backwards all ASICs can be addressed by the Trigger Sorter Master once the μ PU has taken control of the bus A dedicated parallel interface between the μ PU and the TSM has been implemented for this purpose.

At power supply turn-on every Control Board the μ PU starts executing the reset sequence. The boot program, sitting in EPROM, is executed as soon as power voltage stabilizes at nominal value. This program takes care of first hardware diagnostics, checking FLASH and SRAM functionality and power supply bus-bar voltages. After

the self-check the result is sent via slow control link and the μ PU enters a sleep state waiting for remote commands. At this level it is possible to turn on and off any block, to repeat the boot sequence and to access FLASH and SRAM memories for program downloading and execution. Standard program execution foresees the copy of code from FLASH to SRAM and FLASH memory power off for code source protection from SEE. Program execution can take place either in FLASH or in SRAM memory blocks; a separate power supply line allows an independent use of both. On top of program execution a progressive power on sequence is foreseen to allow a full check of mini-crate electronics integrity.

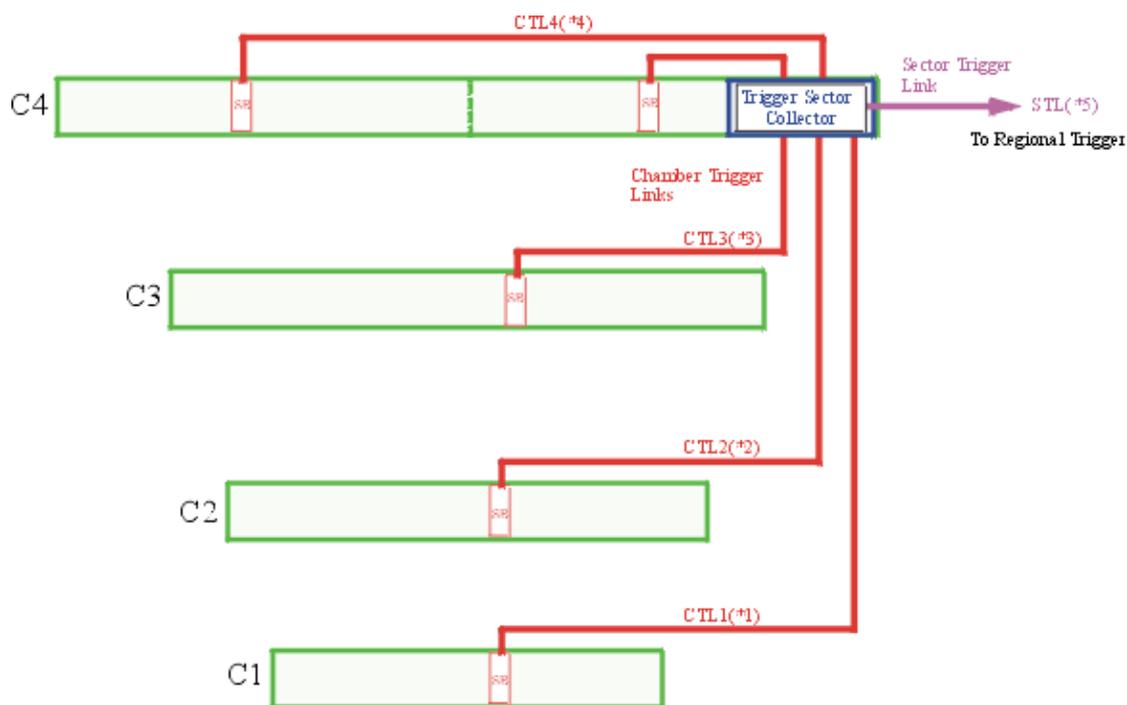
A TTC receiver per mini-crate accomplishes clock and broadcast signals distribution over the barrel drift tubes detector. Every TTC receiver chip delivers two clock lines with programmable fine de-skewing: one is distributed to all Trigger and Readout Boards while the second is used by Server and Control Boards. Broadcast commands are: RESET, LV1A, BCNTRES and the three sequence test commands (SEQTST, SEQRES and SEQADV). RESET performs system reboot, LV1A is the first level trigger strobe, while BCNTRES is the bunch crossing counter reset command that is periodically transmitted for synchronization purposes. TTC programming is done via an I2C interface.

9.7 Sector Collector

The Sector Collector Board (SCB) is lodged in the mini-crate of the fourth station of each sector. All high speed optical links either for readout or for trigger are placed on the SCB. Readout data, coming from each Readout Board on serial medium speed links on twisted pairs, are grouped and formatted to form sector readout packets and sent, via a high speed optical link, to the DAQ.

Readout: Descrizione della formattazione dei dati.

Trigger data, coming from each Server Board on high speed LVDS serial links, are grouped to form sector trigger packets and sent, via a high speed optical link, to



the Regional Trigger (Figure 9.07.01).

Figure 9.07.01: Sketch of SCB connections to Mini-Crate electronics.

The link connecting each SB to the SCB consist of 48-bit LVDS Channel Link Serializer and Deserializer connected by a variable length flat cable with 10 twisted pairs. The device 48 inputs are latched at 40MHz and serialized on 8 twisted pairs at 240Mbit/s; one twisted pair is reserved for clock transmission. The different cable lengths (2m to 4m) compensate, within 2ns, for the different time of flight of particles coming from the vertex and crossing the sector stations. Sector trigger data amount to 164 bits and are transmitted to the Regional Trigger using two PAROLI (Siemens) optical links, one for trigger phi view information and one for theta view information.

A new Sector Collector layout is under study aiming to move the unit out of mini-crate electronics on the balconies. This should allow relaxing device dimensions, power consumption and reliability requirements on trigger optical links thanks to available space and easier access and maintenance. For this new setup, trigger cables from CBs to SCB are much longer and a new transmitter based on LVDS serializers is under test. The possibility to replace the PAROLI optical link with a custom one using a VCSEL array is being evaluated. The 7 Collector Boards of each half wheel are hosted in a crate together to a Balcony Control Board (BCB). The BCB has two serial interfaces, one is intended for test purposes only (called SCI) and one for the detector Slow Control access called SC1. Another connector, called SC2 is provided, for the termination of the RS-485 link connecting all CCB of the half wheel. The SCI is a standard RS-232 running at 9600 baud. The SC1 is an asynchronous serial communication interface with optical connection for full duplex communication between the Master Slow Control (MSC) crate, sitting in Counting Room and balcony crate electronics. A total number of 10 optical links are needed to control electronics lodged on balcony crates.

9.9.2 Latency Determination

Chamber trigger latency can be divided into three contributions: analog signal propagation, trigger computation and digital signal propagation as shown in Figure

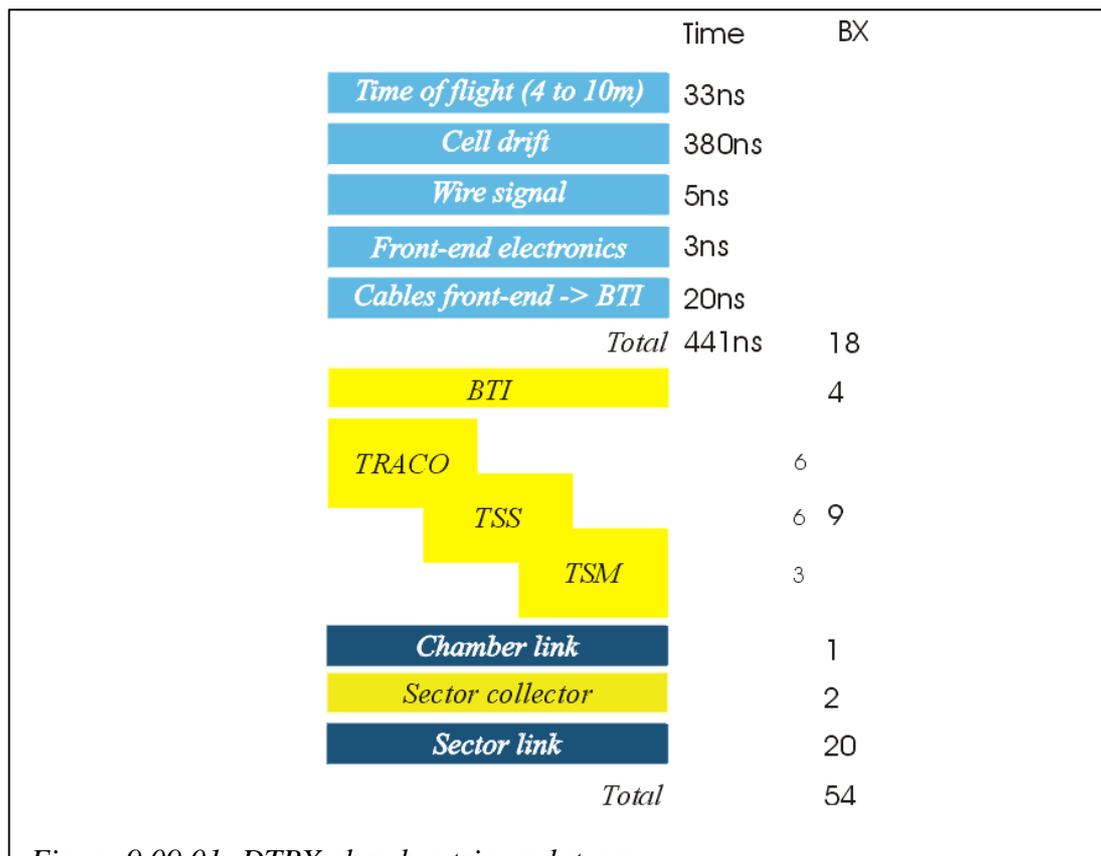


Figure 9.00.01: DTRV chamber trigger latency

9.09.02.

Analog signal propagation consist of particle time of flight from interaction vertex to detector sensitive volume and detector signal propagation up to trigger front-end input (light blue items).

Trigger computation is divided in BTI, TRACO, TSS and TSM parts, including synchronization time needed for detector asynchronous signals sampling (yellow items). TRACO and TSS computations overlap, reducing the sum of the respective latencies to 6 clock cycles.

Digital signal propagation (blue items) includes data transmission from the Server Board to the Sector Collector and from the Sector Collector to the Regional Trigger. Since synchronization of trigger links is accomplished in the Track Finder, using programmable depth FIFOs, length of sector links are at minimum and respective latency is intended as maximum.

9.11.2 TRACO prototype and Test Bench Performance

TRACO prototypes have been designed as standard-cell ASICs using ATMEL 0.5 μ m CMOS technology with three metal layers.