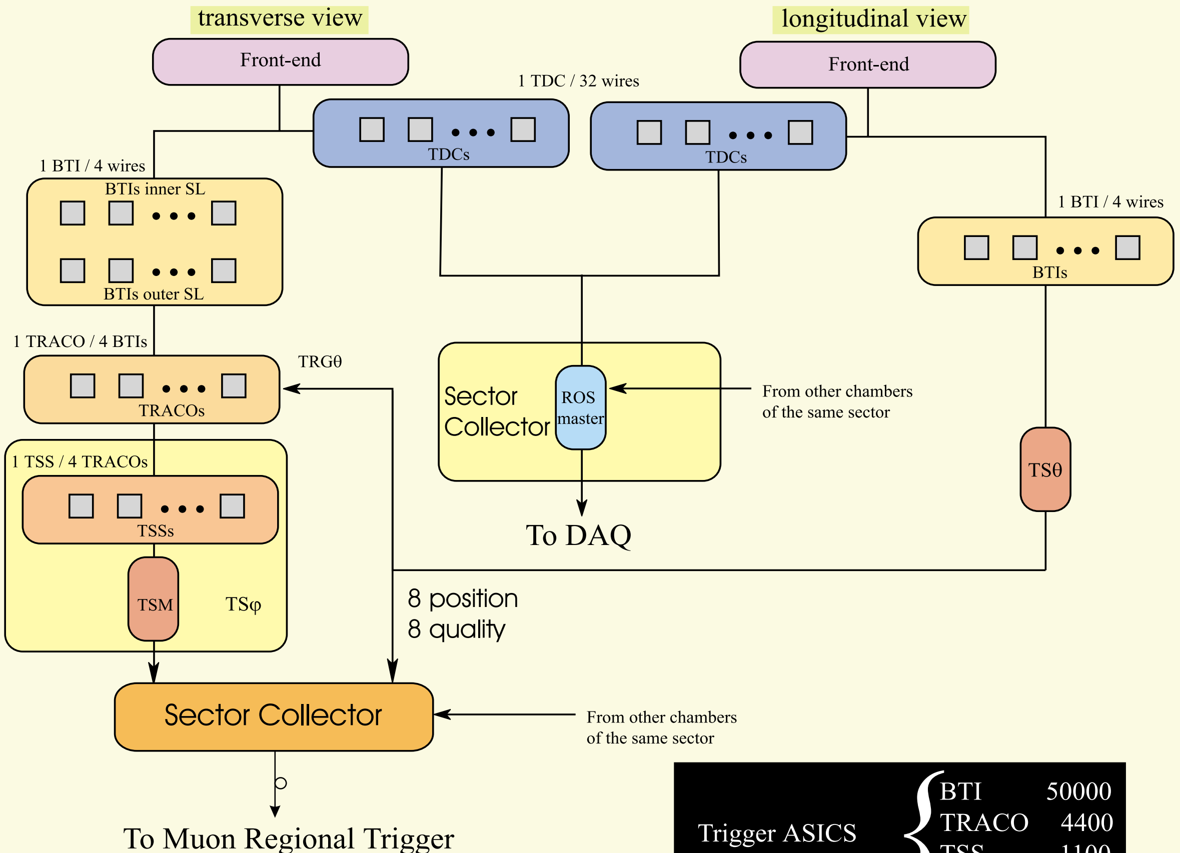
BTI Status

R. Martinelli
I.N.F.N.
Sezione di Padova

05/12/00

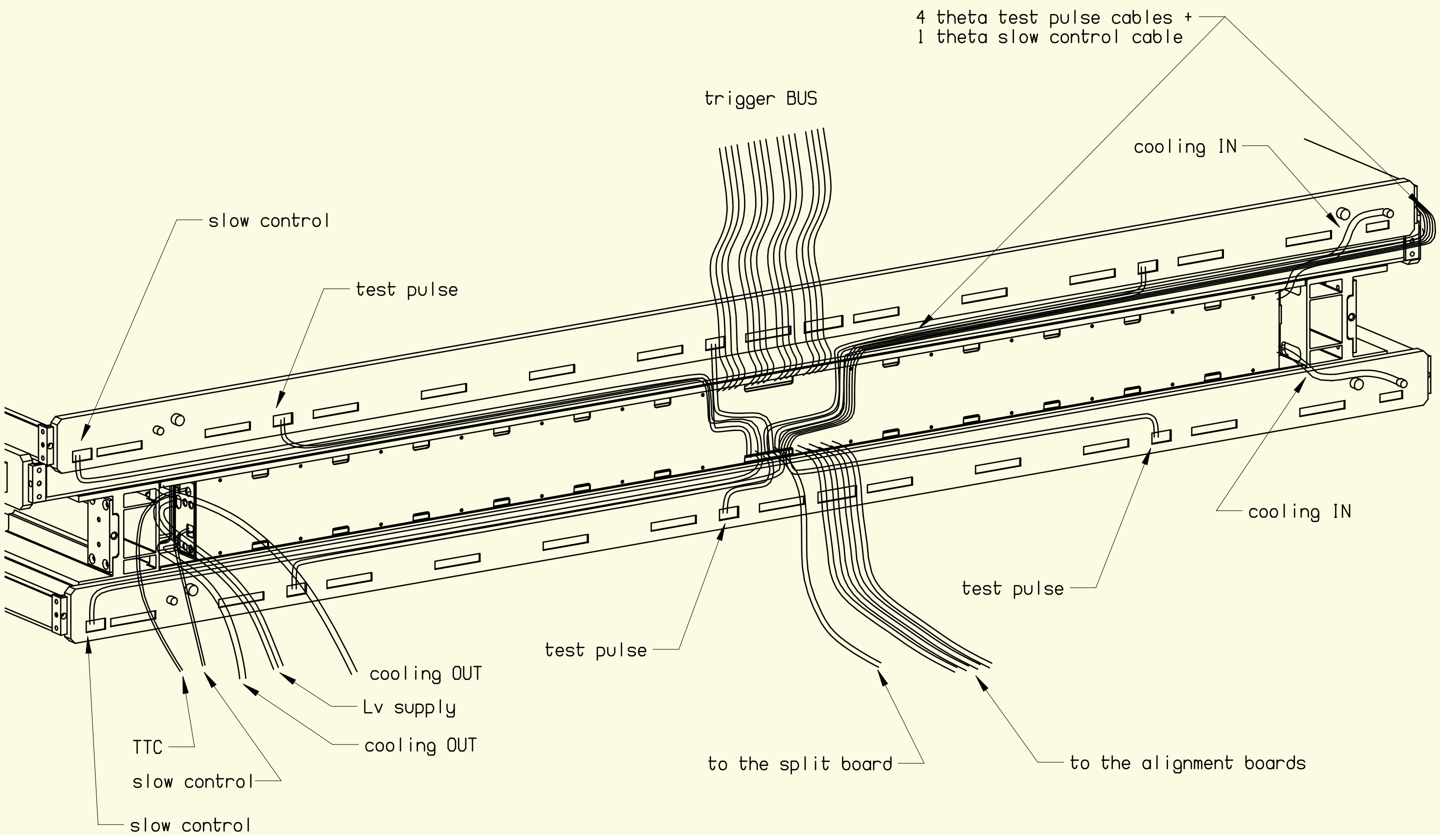
[redacted]

Overview of the electronics layout of a chamber



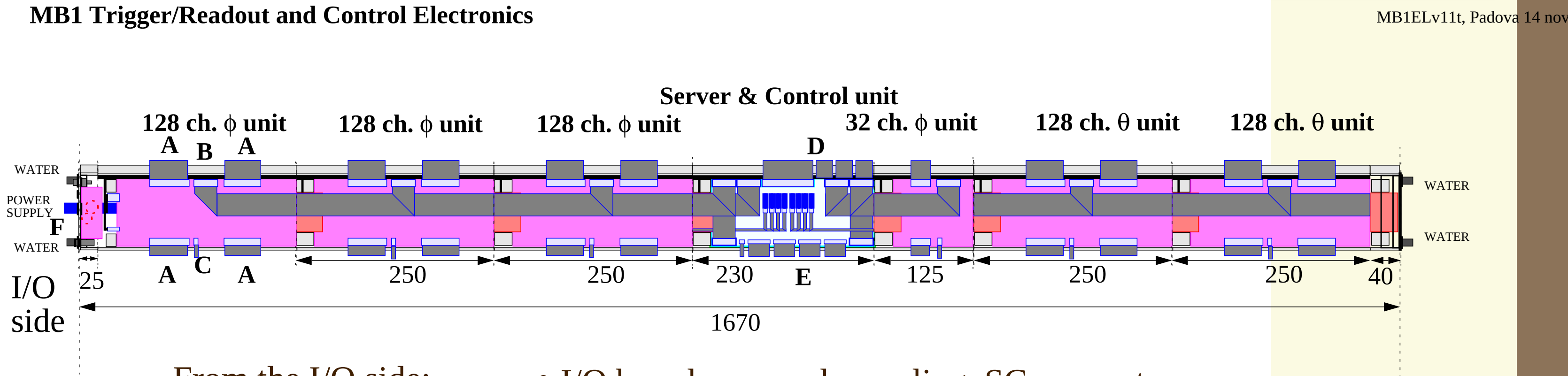
Trigger ASICS		
	BTI	50000
	TRACO	4400
	TSS	1100
	TSM	250

DT Chamber Electronics layout



Trigger R/O minicrate services 990901- signals cables not sketched

DT Chamber Trigger layout



From the I/O side:

- I/O board: power decoupling, SC connectors, …
- three 128 channels Phi_TRB: BTI, TRACO and TSS
- Server and Control board: chamber services, SC interface
- one 32 channels Phi_TRB: BTI, TRACO and TSS
- two 128 channels Theta_TRB: BTI

Each PCB has connections to its neighbours for control signals distribution.
Chamber signals are received via flat cables connecting the ROB to the FE boards (A).
Each TRB sends trigger data to the Server board using a dedicated flat cable (B).
Each ROB is connected to the Sector Collector via a dedicated serial link (C).
The Server and Control unit has connections to chamber electronics (D) for monitoring and control purposes, and connections to the Sector Collector for trigger data transmission (E).

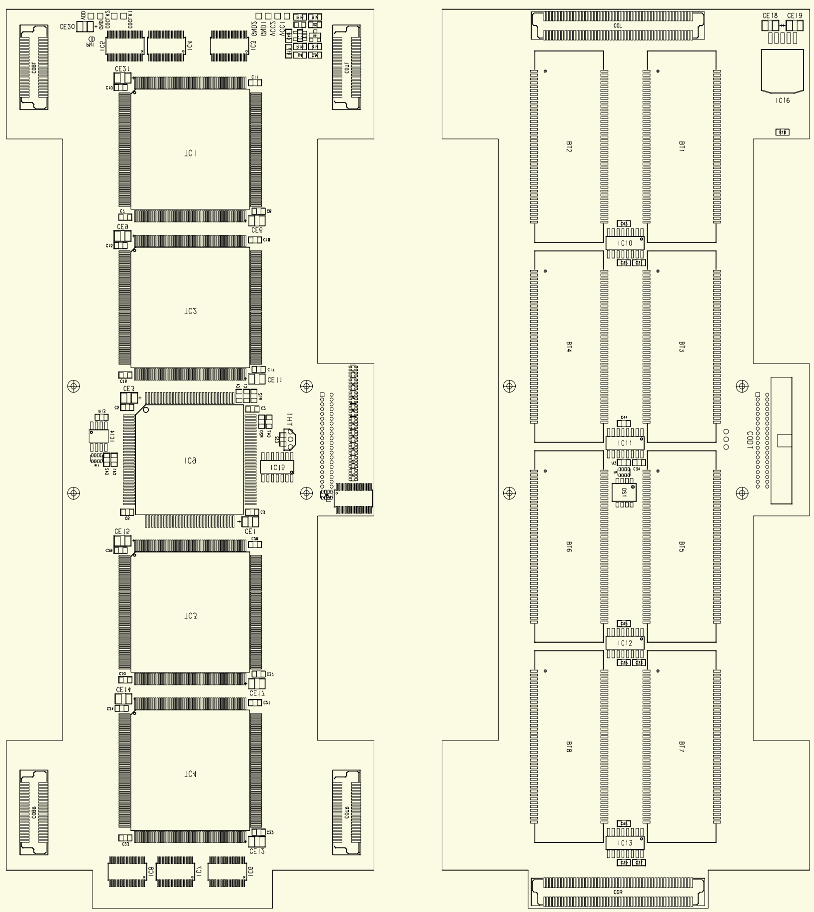
MB1 chamber electronics mini-crate layout

From the I/O side: power supply decoupling
two 128 channels units for the θ view
one 128 channels unit for the ϕ view
the Server and Control unit
two 128 channel units for the ϕ view
one 32 channel unit for the ϕ view

Each 128 channel unit has four flat cables connected to the Front-ends (A)
one flat cable for the Trigger connection with the Server (B)
one twisted pair for the Readout connection with the Sector Collector(C)

The Server and Control unit has connections with the front-ends for settings and monitoring (D),
Trigger connections with the Sector Collector (E) and connections
with the Master Slow Control in the control room (F).

DT Chamber PHI Trigger board

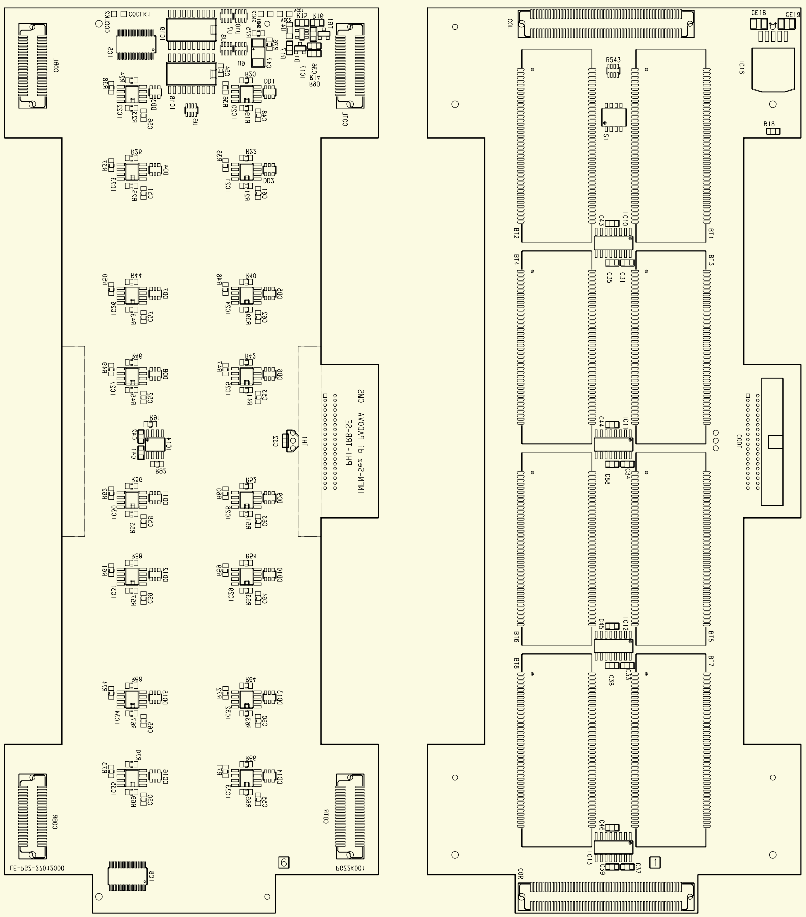


PHI_TRB

- 128 trigger channels
- 3.3V 10W power supply
- 40MHz clock

> 8 BTIM + 4 TRACO + 1 TSS
> single PECL clock input @ 40MHz
> low skew clock distribution
> temperature sensor
> JTAG circuitry
> low-drop regulator with over-voltage and over-current protection
> on/off control and isolation switches

DT Chamber THETA Trigger board



THETA_TRB

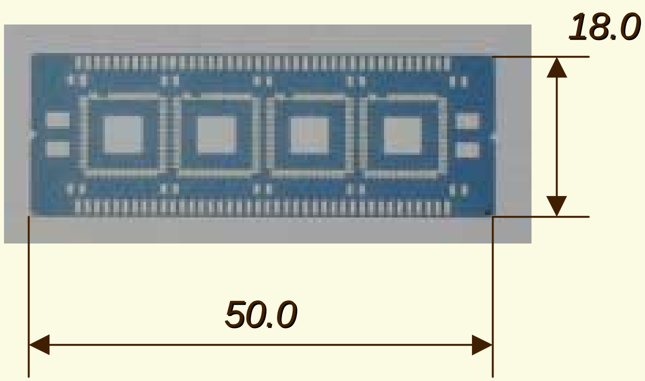
- 128 trigger channels
- 3.3V 10W power supply
- 40MHz clock

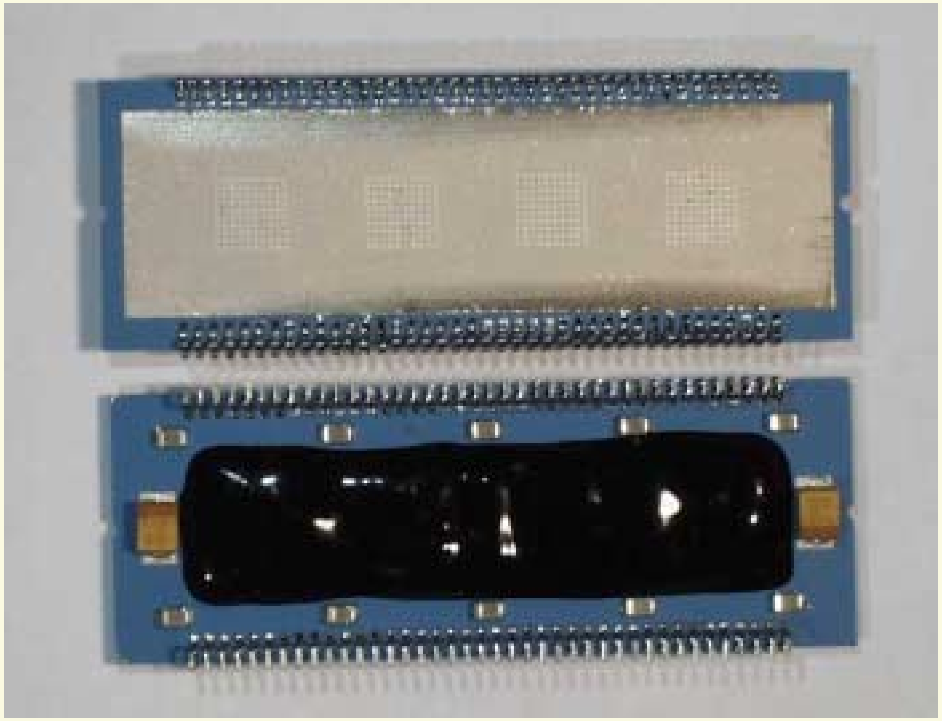
> 8 BTIM
> single PECL clock input @ 40MHz
> low skew clock distribution
> temperature sensor
> JTAG circuitry
> low-drop regulator with over-voltage and over-current protection
> on/off control and isolation switches

BTI Multi-Chip Module

LTCC substrate

- 4 BTI dies
- 3.3V 0.85W
- 80 I/O
- 40MHz and 80MHz clocks





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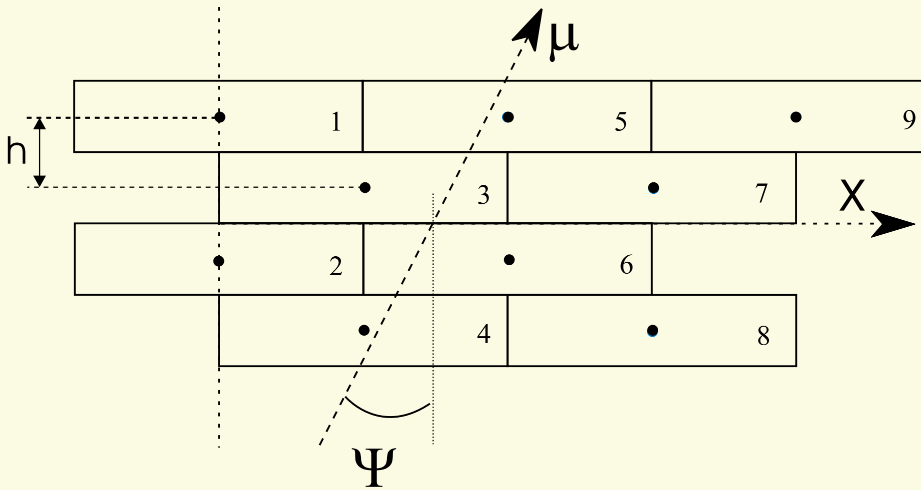

- Detection of single tracks on 9 wires
- Trigger on 3 and 4 out of 4 hit planes with quality flag output
- Track angle and position calculation
- Input signal edge triggered with programmable dead time
- Programmable drift velocity parameter
- Programmable angular acceptance
- Programmable low quality trigger suppression (LTS)
- BIST circuitry and JTAG interface
- Programming via JTAG and Parallel Interface
- 3.3V 250mW, 80MHz sampling clock
- 0.5μm CMOS (ATMEL) with 67k gates and 64 I/O.

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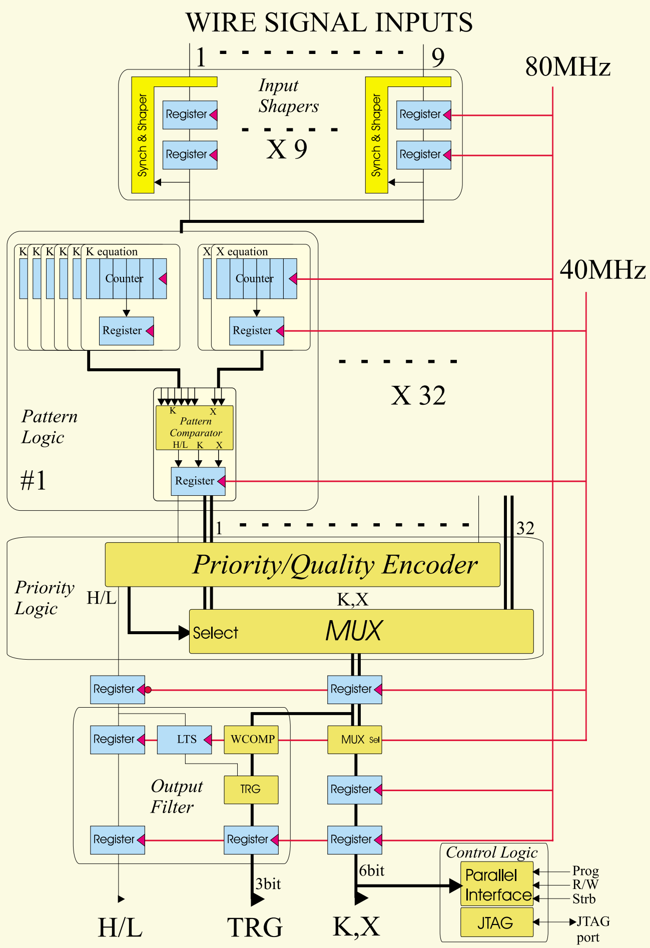

Input signals sampling and shaping at 80MHz

Track pattern detection and impact parameters calculation

Pattern selection

Angular filter and LTS logic

Control logic

BTI: Documents

- Overview and performances of chamber trigger:
  - "Design and Simulations of the Trigger Electronics for the CMS Muon Barrel Chambers", Ist Workshop on Electronics for LHC Experiments, 1995.
- FPGA prototype test:
  - "Beam Test Results of a FPGA Prototype of a Front-end Trigger Device for CMS Muon Barrel Chambers", IInd Workshop on Electronics for LHC Experiments, 1996.
  - "Efficiency studies of the front-end trigger device of the muon drift tubes for the CMS detector at LHC", NIM A 398, 1997.
- Full performance prototype test:
  - "Local Track Reconstruction for the First Level Trigger in the CMS Muon Barrel Chambers", IVth Workshop on Electronics for LHC Experiments, 1998.
  - "Test results of the ASIC front-end trigger prototypes for the muon barrel detector of CMS at LHC", NIM A 438, 1999.
  - "Current knowledge of BTI performance in magnetic field", CMS Note 2000/044.

BTI Performance: efficiency

Efficiency at normal incidence for different synchronization acceptance windows

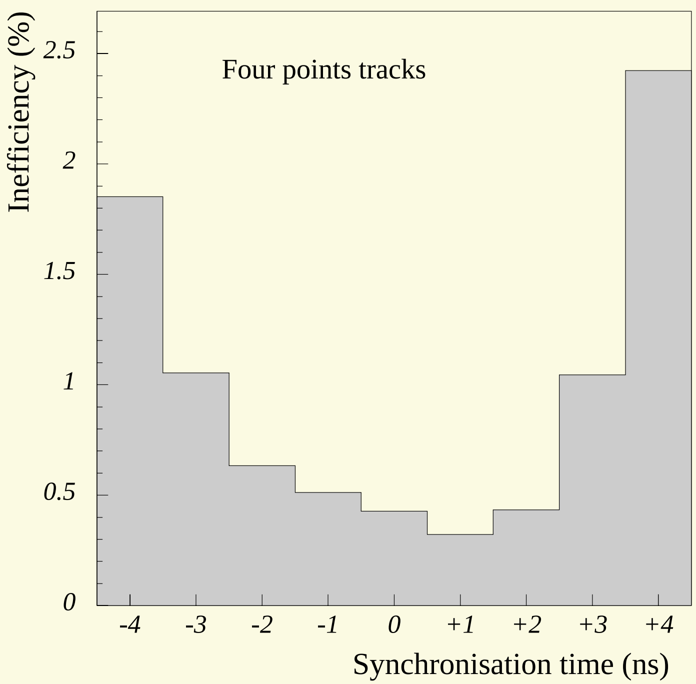

Figure 5

Synchronization range	±2ns	±4ns	±6ns	±8ns	±10ns	±12ns
HTRG fraction	84.3%	83.0%	81.7%	79.0%	75.0%	70.5%
LTRG fraction	14.5%	15.4%	16.7%	19.4%	23.3%	27.8%
Efficiency	98.8%	98.5%	98.5%	98.5%	98.3%	98.3%

Table 1 – BTI performance for different synchronization accept

BTI acceptance	LTS	HTRG fraction	LTRG fraction	Inefficiency
Standard	[illegible]	[illegible]	[illegible]	0.3%
Standard	[illegible]	[illegible]	[illegible]	1.3%
Minimum	[illegible]	[illegible]	[illegible]	1.1%
Maximum	[illegible]	[illegible]	[illegible]	1.4%

Table 2 – E [illegible] ed configurations

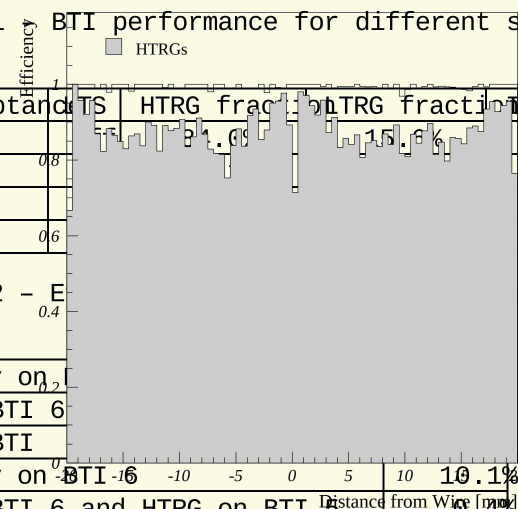

Figure 10

HTRG only on [illegible]	[illegible]
HTRG on BTI 6 [illegible]	[illegible]
HTRG on BTI [illegible]	[illegible]
LTRG only on BTI 6	10.1%
LTRG on BTI 6 and HTRG on BTI 5	0.4%
LTRG on BTI 6 and LTRG on BTI 5	5.9%

Table 3 – Probability of a redundancy trigger in adjacent BTI

BTI acceptance	LTS	%H out of time	%L out of
Standard	off	[illegible]	[illegible]

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BTI Performance: efficiency

Efficiency and noise versus track incidence angle

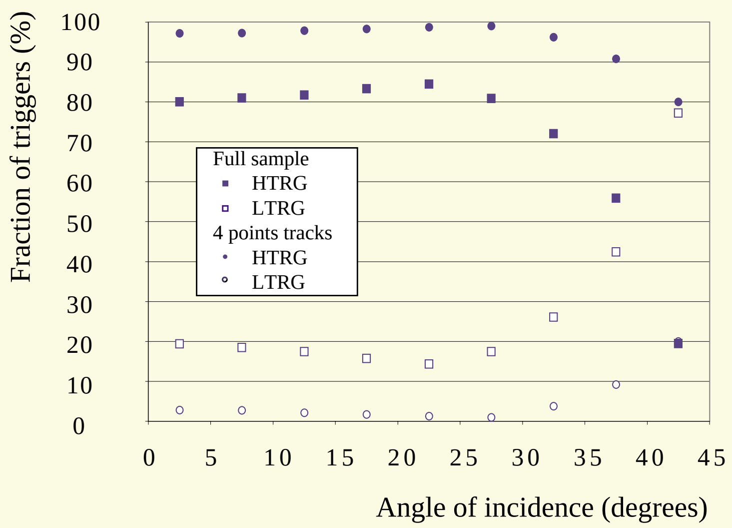


Figure 11

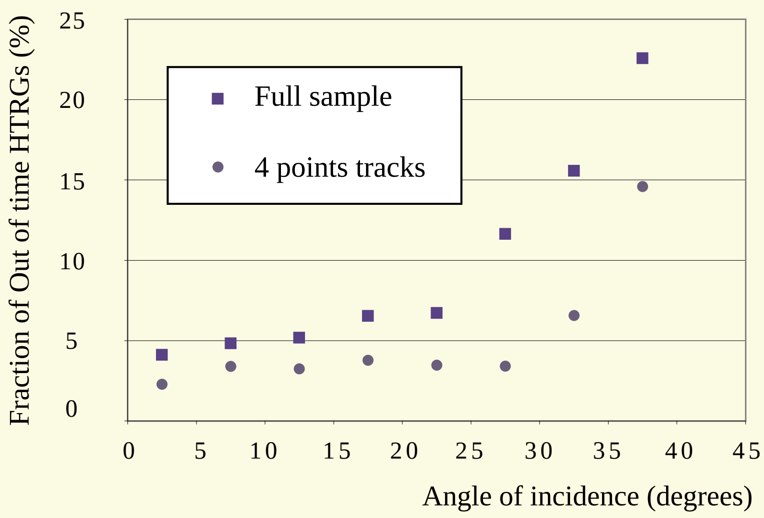


Figure 12

BTI Performance: efficiency

LTRG fraction	14.5%	15.4%	16.7%	19.4%	23.3%	27.8%
Efficiency	98.8%	98.5%	98.5%	98.5%	98.3%	98.3%

Efficiency for different configurations

Table 1 – BTI performance for different synchronizatio

BTI acceptance	LTS	HTRG fraction	LTRG fraction	Inefficiency
Standard	off	84.0%	15.6%	0.3%
Standard	on	85.1%	13.6%	1.3%
Minimum	on	70.7%	28.2%	1.1%
Maximum	on	84.8%	13.8%	1.4%

Table 2 – Efficiency figures for the tested configurati

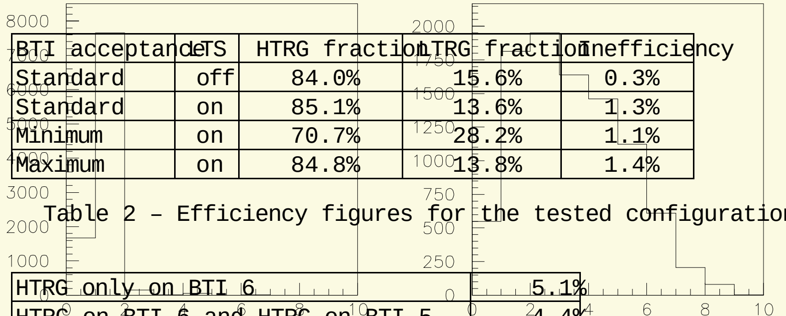
HTRG only on BTI 6	5.1%
HTRG on BTI 6 and HTRG on BTI 5	4.4%
HTRG on BTI 6 and LTRG on BTI 5	74.0%
LTRG only on BTI 6	10.1%

BTI Performance: bx identification

BX Efficiency and noise

Synchronization range	±2ns	±4ns	±6ns	±8ns	±10ns	±12ns
HTRG fraction	84.3%	83.				
LTRG fraction	14.5%	15.				
Efficiency	98.8%	98.				

Table 1 – BTI performance for different synchronization acceptance windc



BTI acceptance	LTS	HTRG fraction	LTRG fraction	Inefficiency
Standard	off	84.0%	15.6%	0.3%
Standard	on	85.1%	13.6%	1.3%
Minimum	on	70.7%	28.2%	1.1%
Maximum	on	84.8%	13.8%	1.4%

Table 2 – Efficiency figures for the tested configurations

HTRG only on BTI 6	5.1%
HTRG on BTI 6 and HTRG on BTI 5	4.4%
HTRG on BTI 6 and LTRG on BTI 5	74.0%
LTRG only on BTI 6	10.1%
LTRG on BTI 6 and HTRG on BTI 5	0.4%
LTRG on BTI 6 and LTRG on BTI 5	5.9%

Table 3 – Probability of a redundancy trigger in adjacent BTI

Figure 13

BTI acceptance	LTS	%H out of time	%L out of time
Standard	off	3.0%	351.2%
Standard	on	3.1%	148.2%
Minimum	on	1.1%	175.6%
Maximum	on	4.1%	165.3%

Table 4 – Average fraction of out of time triggers

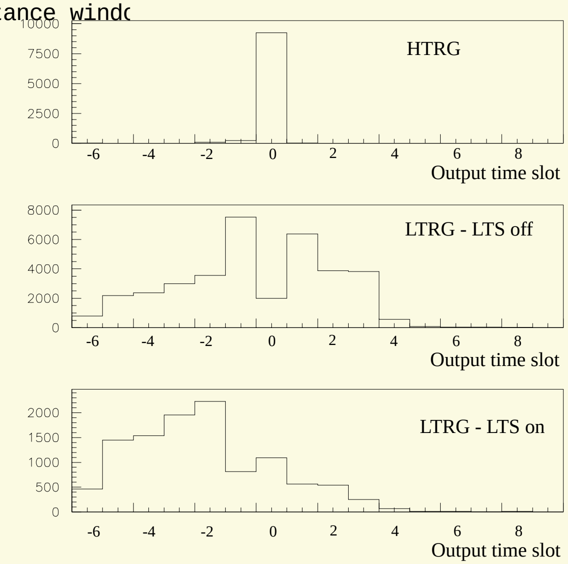
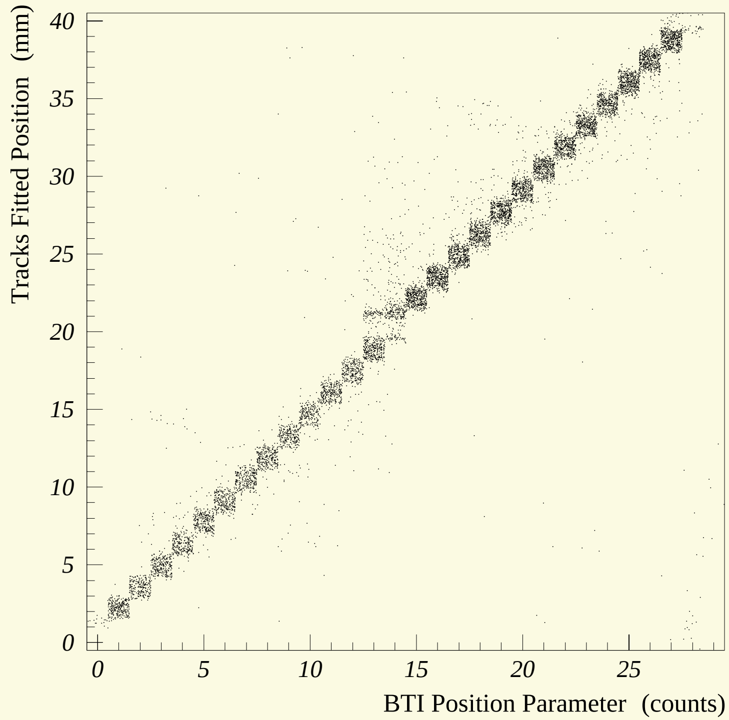


Figure 16

	%HTRG	%LTRG	Inefficiency	%H out of time	%L out of time
No Radiation	84.0%	15.6%	0.3%	3.0%	351.2%
Radiation 10 Hz/cm²	83.0%	16.6%	0.5%	2.5%	800.0%

BTI Performance: position measurement

Accuracy of track position measurement



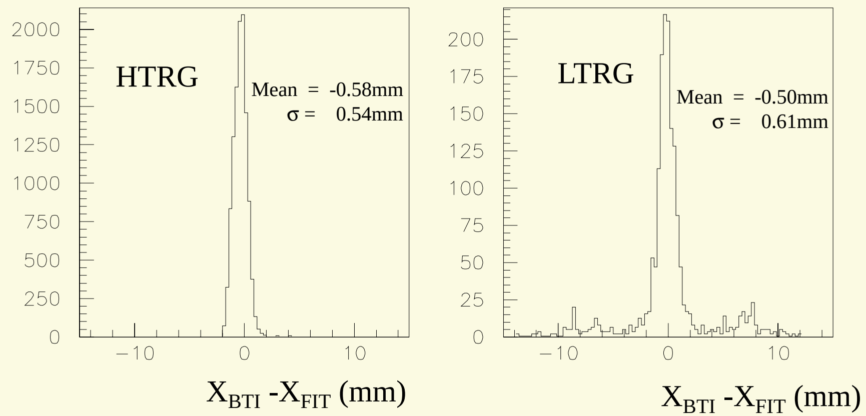
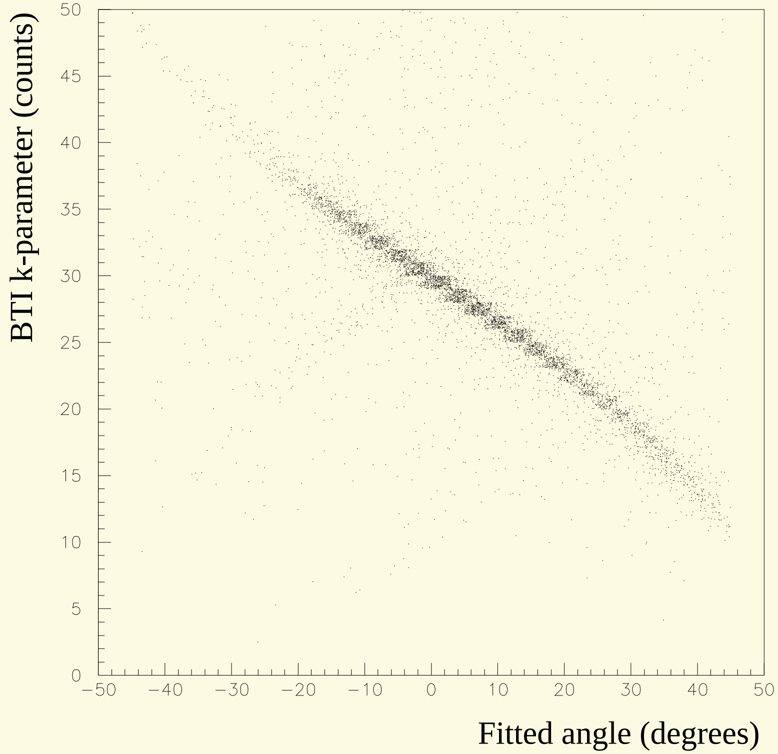


Figure 7

Figure 6

BTI Performance: angle measurement

Accuracy of track angle measurement



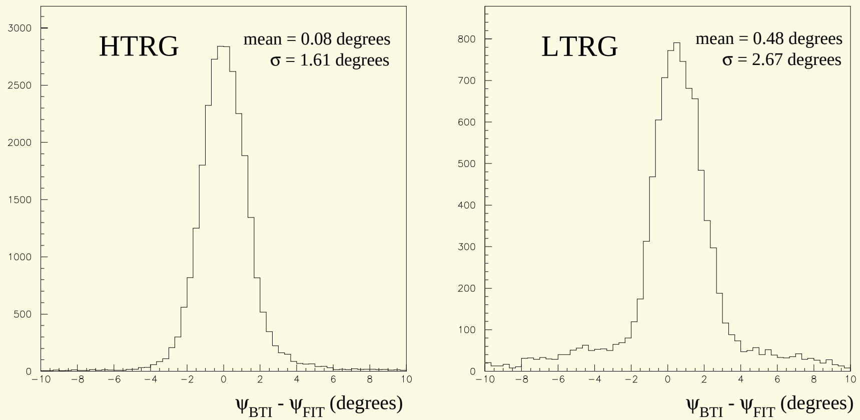


Figure 9

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Figure 8

BTI Performance: magnetic field

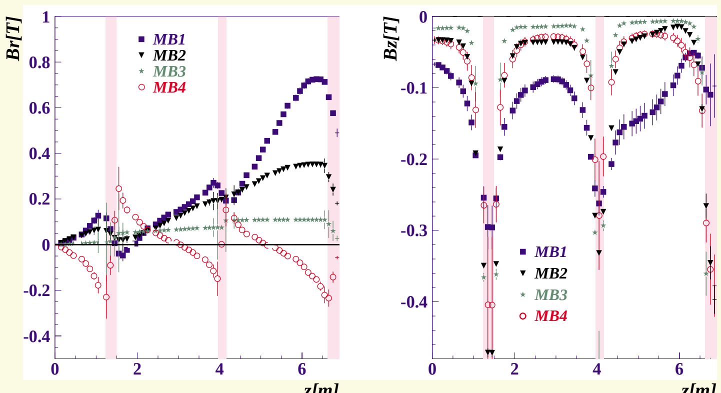


Figure 15- Expected magnetic field components in CMS. B_r is the radial component and B_z is the longitudinal one

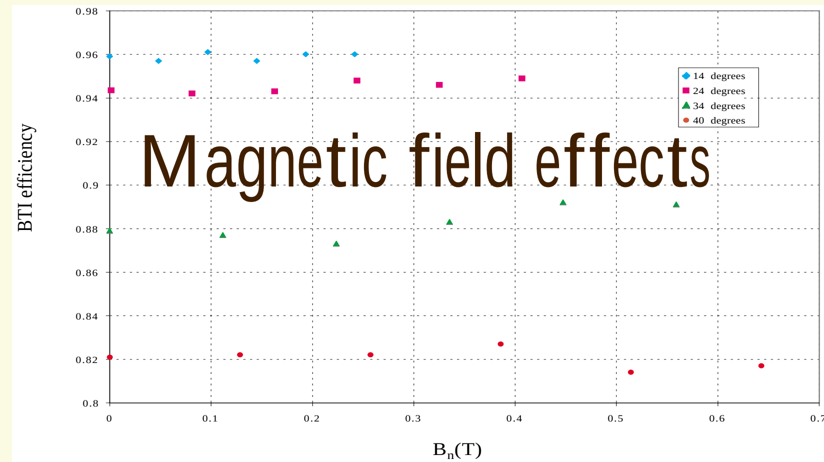


Figure 21- BTI efficiency as a function of B_n in presence of a B_E component.

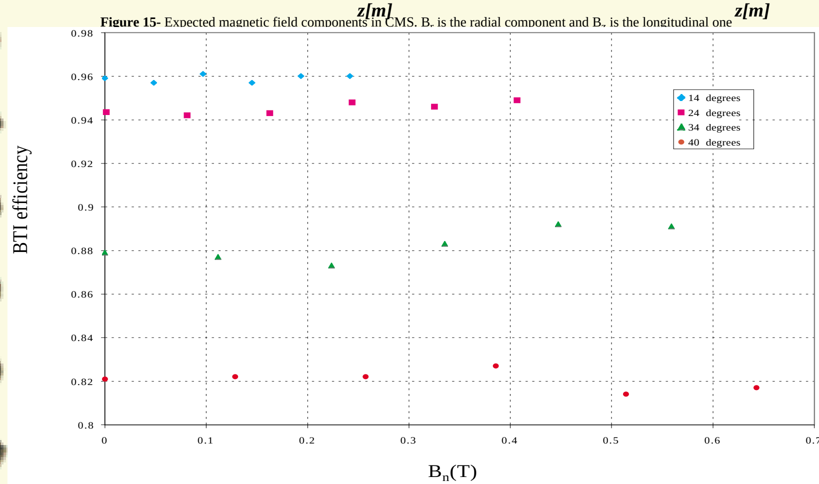


Figure 21- BTI efficiency as a function of B_n in presence of a B_E component.

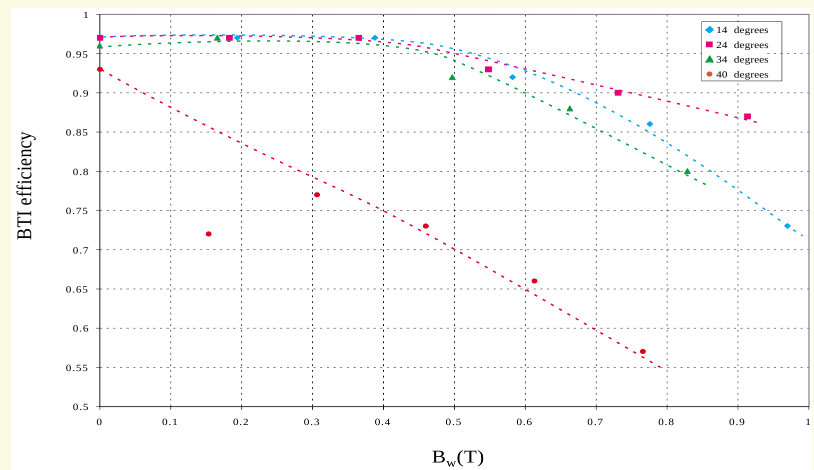
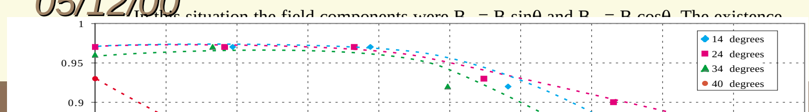


Figure 22- BTI efficiency as a function of B_w in presence of a B_n component.

5.2.3 **Performance under mixed (B_n, B_E)**

In this situation the field components were $B_n = B \sin\theta$ and $B_E = B \cos\theta$. The existence



BTI Performance: gamma rays background

Gamma rays background affects track position accuracy

Gamma rate = 10Hz/cm^2

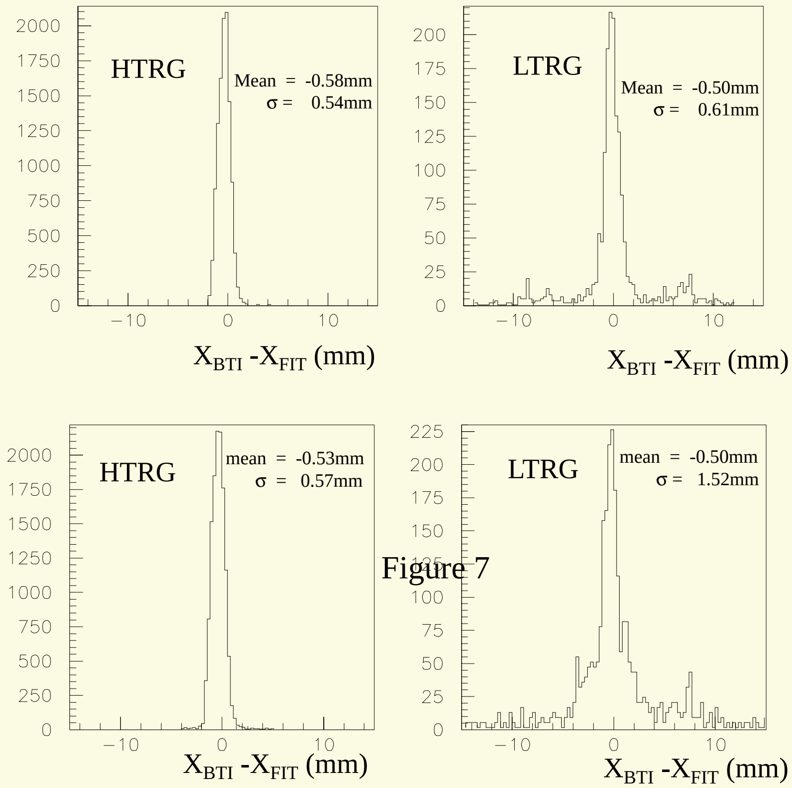


Figure 7

With gamma rays background

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Figure 18

BTI Performance: gamma rays background

LTRG on BTI 6 and HTRG on BTI 5	0.4%
LTRG on BTI 6 and LTRG on BTI 5	5.9%

Table 3 – Probability of a redundancy trigger in adjacent BTI

Gamma rays background affects efficiency

BTI acceptance	LTS	%H out of time	%L out of t
Standard	off	3.0%	351.2%
Stan	[illegible]	[illegible]	148.2%
Minim	[illegible]	[illegible]	175.6%
Maximum	on	4.1%	165.3%

Table 4 – Average fraction of out of time triggers

Gamma rate = 10Hz/cm^2

	%HTRG	%LTRG	Inefficiency	%H out of time	%L out of time
No Radiation	84.0%	15.6%	0.3%	3.0%	351.2%
Radiation 10 Hz/cm^2	83.0%	16.6%	0.5%	2.5%	800.0%

Table 5 – Comparison between performance without radiation and m

BTI Performance: neutron tolerance

VIII. RESULTS SUMMARY

Results of the various tests are collected in Table 3 considering only the worst result for each device. We quote a 90% confidence level upper limit of the SEU cross section for all the integrated circuits which experienced no failure. The error in the SRAM SEU cross section is the squared sum of statistical and systematical error. The latter one is due to the uncertainty of the total neutron flux and is dominating our calculation. The Mean Time Between Failures is computed for the whole barrel muon detector, considering the numb... chip used in the electronics layout. W... BTI chips and few hundred pieces of t...

[3] D.L. Oberg et al., IEEE Trans. On Nucl. Science, vol.43, No.6, Dec 1996

[4] P.J. Griffin et al., IEEE Trans. On Nucl. Science, vol.44, No.6, Dec 1997

[5] E. Normand, IEEE Trans. On Nucl. Science, vol.45, No.6, Dec 1998

[6] K. Johansson et al., IEEE Trans. On Nucl. Science, vol.45, No.6, Dec 1998

[7] J. W. Meadows, NIM. A324(1993)239.

D.L. Smith et al.,NIM A241(1985)507.

l., Advances in Neutron Capture Therapy,

l, Rad. Prot. Dos., Vol. 70, p. 559 (1997)

Neutron tolerance

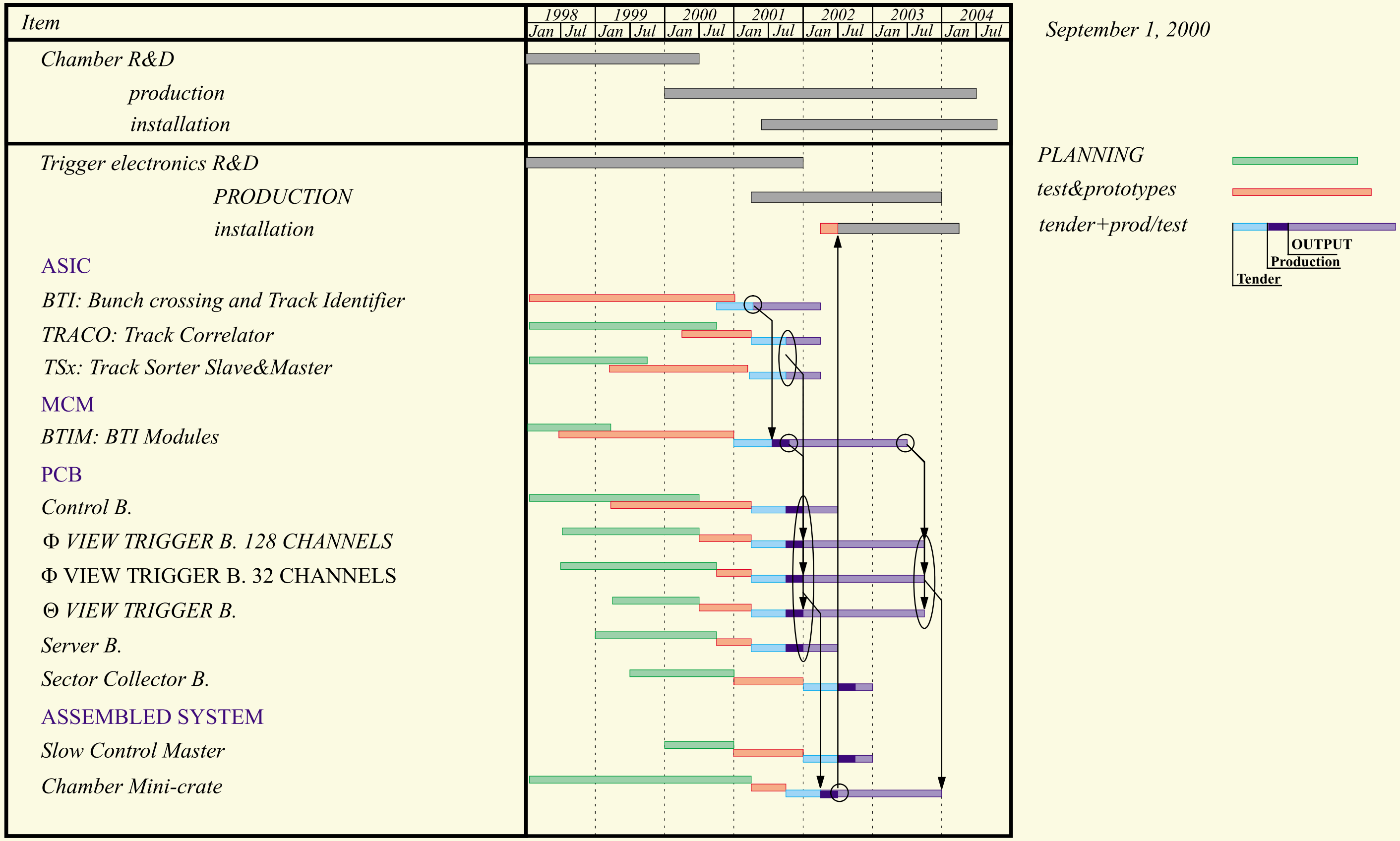
Table 3: SEU cross section and expected mean time between failures in the whole CMS muon barrel detector due to neutrons of different energy. We considered 500 n/cm^2 of thermal neutrons, 20 n/cm^2 with $3<E_n<10$ MeV and 30 n/cm^2 with $E_n>10$ MeV.

	SEU cross section (cm^2)			Mean Time Between Failures (hours)		
Device	Thermal	LNL	UCL	Thermal	LNL	UCL
LD reg	$< 1.38\times10^{-10}$	$< 1.40\times10^{-11}$	$< 1.00\times10^{-12}$	< 64	< 15587	< 147892
μP	$< 1.38\times10^{-10}$	$< 1.40\times10^{-11}$	3.85×10^{-11}	< 385	< 95340	23088
FLASH	$< 1.38\times10^{-10}$	$< 1.46\times10^{-12}$	$< 1.00\times10^{-12}$	< 385	< 91101	< 474734
SRAM	$(1.13\pm0.2)\times10^{-9}$	$(7.03\pm0.2)\times10^{-10}$	$(1.03\pm0.2)\times10^{-8}$	23.5	1263	23
EPROM	$< 1.38\times10^{-10}$	$< 1.61\times10^{-11}$	$< 1.00\times10^{-12}$	< 385	< 83043	< 474734
Optolink	$< 1.38\times10^{-10}$	$< 1.43\times10^{-11}$	$< 1.00\times10^{-12}$	< 385	< 93231	< 474734
ASIC TSS	$< 2.68\times10^{-10}$	$< 9.46\times10^{-12}$		< 33	< 32225	
ASIC BTI	$< 1.75\times10^{-10}$	$< 1.31\times10^{-11}$	$< 1.00\times10^{-12}$	< 1.5	< 507	< 4436

No measurable degradation was observed after 10^{12} n/cm^2.
No SEE were observed.

SCHEDULE OF CHAMBER TRIGGER AND CONTROL ELECTRONICS

CESV10E, PADOVA 18 FEB 2000



05/12/00

BTI: Project Status

- BTI and DT chamber prototypes tested:
  - with muon beams and cosmic rays
  - with muon beams and radiation background (GIF)
  - with muon beams in high magnetic fields
- BTI tests in radiation background:
  - 10krad in gamma cell (2krad/minute)
  - thermal neutrons up to 10^{10} n/cm^2
  - fast neutrons from reactor (Prospero) up to 10^{11} n/cm^2
  - fast neutrons (< 10MeV) from d-Be reaction up to $2x10^{12}$ n/cm^2
  - fast neutrons (< 60MeV) from p-Be reaction up to 10^{12} n/cm^2

Functional behaviour and performance are fully satisfactory.

After irradiation tests up to the reported levels no degradation in the electrical or functional characteristics was measured. No SEE was observed.

BTI: Project status and future developments

- *Status and known problems:*
  - The ATMEL foundry in Europe has been closed. Only 1400 dies are still available from the first prototyping batch. The next batch could be produced by ATMEL in USA after a new prototyping phase and with 30 weeks of mask processing time.
  - BTIM prototypes with LTCC substrate have low yield, about 40%.
- *Future developments:*
  - The BTI/BTIM tender must start as soon as possible to account for the unexpected delay needed by ATMEL to start chip production. A new prototyping batch could be received within mid 2001 placing the order for BTI production in December 1999.
  - In order to gain time for BTIM production the tender must be anticipated and the 1400 available dies must be used for further prototyping.
  - BTIM production schedule:
    - 50 pcs by September 2001
    - 950 pcs by December 2001
    - 5 lots of 2300 pcs from March 2002 to June 2003.