CMS - PADOVA

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DRAFT

Track Correlator

User manual

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1. Introduction

The proposed baseline of the DTBX chamber trigger is a multistage scheme.

The front-end trigger device is called Bunch and Track Identifier (BTI)[1]: it performs a rough track reconstruction and uniquely identifies the parent bunch crossing of the candidate track by means of a generalized mean-timer technique. First prototypes were already produced.

The BTI is followed in the electronics chain by a Track Correlator (TRACO) that is required to associate portions of tracks in the same chamber relating predefined groups of BTIs among them.

A third device, called Trigger Server[2], performs the track selection within a full chamber and forwards information to the Muon Regional Trigger[3], that finally extracts the track candidate transverse momentum.

2. Short Description of BTI

The Bunch and Track Identifier was studied to work on each groups of four layers of staggered drift tubes called Super Layers (SL), aiming to the identification of the tracks giving a signal in at least three of the planes. We quickly recall the basic description of the device: any other detail can be found in Reference 4.

Each BTI is connected to nine wires allocated as shown in Figure 1.

The parameters computed from the BTI are the angular k-parameter $k = h \tan \psi$ (the track direction) and the crossing position, computed in the SL central plane. The geometrical quantities involved are shown in Figure 1: ψ is the angle of the track with respect to the normal to the chamber and $h = 1.3mm$ is the distance between the wire planes.

These parameters are evaluated by means of a generalized mean-timer technique: this method is a search inside a BTI for the alignments of the recorded hits belonging to a track. If there is an alignment of four hits the signal is marked as High Quality Trigger (HTRG), while if it is due to the alignment of only three hits, it is marked as Low

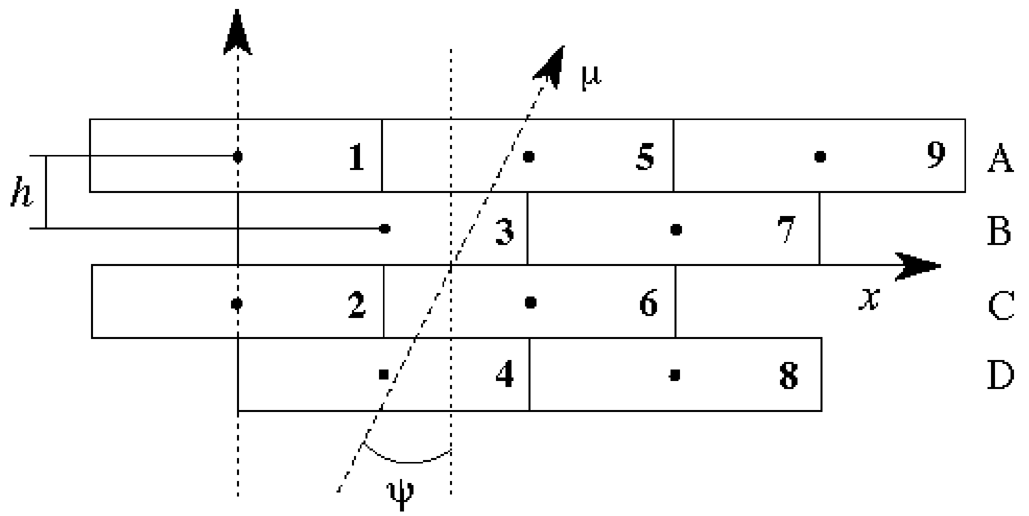

Figure 1 - BTI layout showing channels allocation.

Quality Trigger (LTRG).

The alignment occurs with fixed delay with respect to the parent bunch crossing time, thus permitting its identification. The total latency of the BTI is determined by the maximum drift-time to the wires, T_{MAX}, plus 4 clock cycles needed for input signal synchronization and BTI calculations. For a nominal drift velocity of 50 μm/ns the delay of the TRG signal with respect to the parent interaction is therefore 20 bunch crossings.

The BTI trigger algorithm actually generates HTRGs and LTRGs when the computed k-parameters of any of the predefined patterns of wires are equal within the programmed tolerance. The definition and the full list of the preloaded patterns is available in Reference 4.

Position and angular resolution of the device depend on the drift velocity and on the sampling frequency of the device. For a nominal drift velocity of 50 μm/ns and a sampling frequency of 40 MHz, the angle is measured with a resolution better than 60mrad, while the position is measured with a resolution of 1.25mm. The angular resolution is track pattern dependent and is generally worse for LTRGs.

Using the current geometric parameters of the chamber, as described in version 113 of the CMS detector sofware, the angular acceptance is nominally $\psi_{MAX} = \pm 55°$.

Each SL is equipped with one BTI every four wires and the BTIs are overlapped by five wires assuring that every track, with angle within the maximum acceptance range, is fully contained in at least one BTI.

K-parameter and position of the track as measured from the corresponding equations, coded in 6 bits, and one trigger quality bit, marking HTRG or LTRG (H/L), are transmitted to the TRACO on the BTI track-data bus.

Only one track per bunch crossing per BTI is forwarded to the TRACO.

3. Track Correlator layout

The DTBX chamber is composed of two SL in the CMS transverse plane (φ view) and one SL in the longitudinal one (θ view). Each SL is equipped with BTIs.

The TRACO is a processor that interconnects the two SL of the transverse plane. It receives the information from the BTI devices connected to it and tries to find the couple of BTI track segments that fits the best track, linking the inner layer candidates

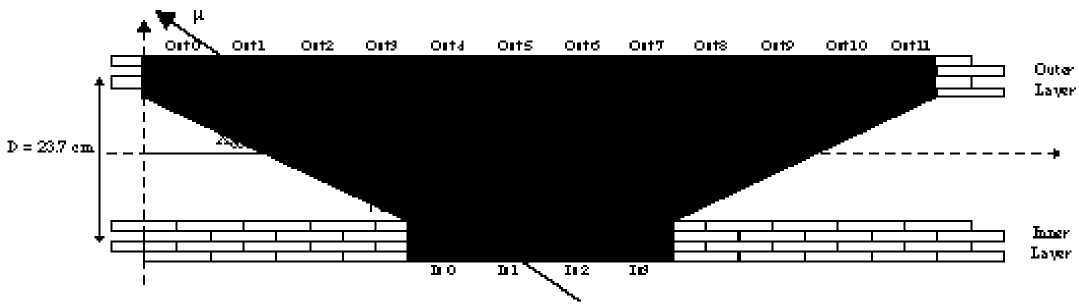

Figure 2 - Track Correlator layout

to the outer layer ones.

The number of BTIs connected to a TRACO is limited from the size of the chip and it is determined by the acceptance requirement. The final design connects four BTIs of the inner Superlayer to twelve BTIs of the outer Superlayer allocated as shown in Figure 2.

The introduction of this device is necessary since the BTI is intrinsically a noisy device and therefore a local preselection and a quality certification of the BTI triggers is required. Furthermore the number of BTIs per chamber is around few hundreds and it is not possible to connect together all the channels to perform any preselection at chamber level.

4. Track Correlator Specifications

The block diagram of the TRACO operations is given in Figure 3. In the following paragraphs we shall describe the TRACO algorithm referring to the flow of this diagram.

4.1 Data paths

In order to allow the identification of two muons inside the same correlator, the TRACO algorithm is applied twice to the data received from the BTI. Therefore inside the TRACO there are two parallel flows delayed by one cycle: the first path computes a First Track, choosing between all the BTI candidates, while the delayed path computes a Second Track from all unused candidates. The programmability of the preferences for the choice of the First Track and the Second Track are completely independent, although in principle we believe that the same criteria should apply.

Inside the full system a further selection is needed in the case that more than one TRACO inside a chamber give a trigger. The communication between the TRACOs and the chamber trigger server to allow this decision is done using a dedicated PREVIEW data bus for each track, in order to minimize the time needed for calculations of the whole trigger chain. A copy of the converted angle (see paragraph 4.3) of one of the candidates chosen for correlation is sent to the Trigger Server according to the programmed H/L and IN/OUT selection flags, as soon as the correlation calculation has been performed. The Trigger Server selection is based on the quality of the PREVIEW of the various candidates. The preview data is composed by 9 bits: five bits for the module of the converted angle, one bit for the track quality (H/L); one bit identifying First/Second track; one bit identifying Inner/Outer layer; one bit identifying Correlated/Uncorrelated track candidate.

4.2 Input Register (16 x 8bits)

This register receives and latches the data values and the qualification flags from the BTI chip. The TRACO collects the inputs from 16 BTIs (four from the inner layer and twelve from the outer layer).

From each BTI the input data bus contains the k-parameter and the position in the BTI coordinate system, multiplexed at 80MHz on the same lines (6 bits wide). Two extra flags are provided: the trigger quality (H/L) and the strobe. TRACO inputs latch

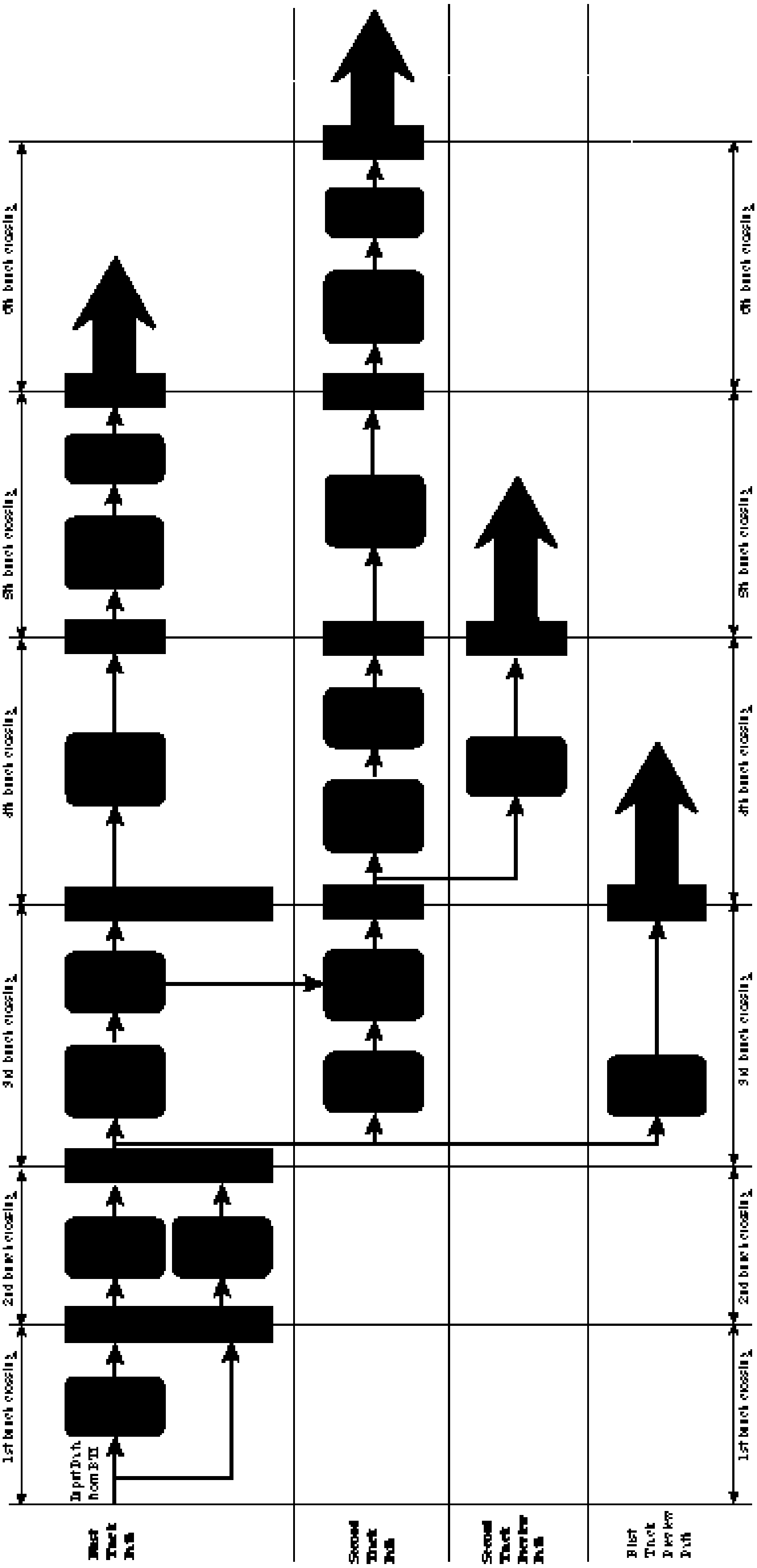

Figure 3 - TRACO Block Diagram

the k-parameter on the rising edge of clock and the position on the next falling edge. (timing ?)

4.3 Angle and position converter

This module receives the k-parameter 6 bits input word from the BTI and converts it into local radial coordinates

$$k_{local} = k_{BTI} - RAD - BTIC$$

The RAD parameter is a 5 bits programmable value, depending on the geographical position of the correlator, i.e. the k-parameter of radial tracks passing through its center. The BTIC is a 6 bits programmable value dependent on the maximum drift time the BTI is programmed for: BTI k parameter has an offset equal to the programmed maximum drift time (ST parameter); meaning that orthogonal tracks have k value equal to ST. The converted angle is used for internal calculations and sent on the Preview bus to the Trigger Server for further track selection.

Each BTI position is converted to TRACO position, offsetting by the appropriate geographical value. An additional Superlayer shift parameter is provided to correct for eventual construction misalignments of the two quadruplets: a programmable 6 bits value IBTIOFF is added to inner positions.

4.4 Sorter

This module receives the converted angle and selects the candidate with the smallest angle,i.e. the angle closest to the local radial direction. There are two sorters for the four inner BTIs and two for the twelve outer BTIs, in order to select the two best candidates for the first track and for the second track in pipeline. The choice is done twice independently on the two φ Superlayers.

The sorting operation can be programmed to select the biggest angle (FHISM and SHISM) instead of the smallest one, and/or to give preference to candidates tagged with the HTRG quality flag (FHTPRF and SHTPRF).

4.5 Calculator and Comparator

This module computes the k-parameter and the position of the correlated candidate. It transforms the inner and outer k-parameter of the two independently selected track segments into the correlator coordinates system and computes the correlated track parameters.

The internal parameters computed for the correlated tracks are:

$$\begin{cases} k_{COR} = \dfrac{D}{2}\tan\psi = x_{inner} - x_{outer} \\ x_{COR} = \dfrac{(x_{inner} + x_{outer})}{2} \end{cases}$$

where D is a 5 bits value representing the ratio of the distance between the two Superlayers and the distance of two wire planes in a Superlayer. Only three values are allowed: 16, 18 and 20. The angular resolution of a correlated track candidate is 10mrad for the nominal drift velocity, thus improving the BTI value by almost an order of magnitude, while the resolution on the position is unchanged.

A second step compares the k parameter of inner track, outer track and correlated calculation. If the correlated value fits inside the programmed acceptance window (FPRGCOMP<1:0> and SPRGCOMP<1:0> for first and second track candidates respectively) with respect to the parent segments the correlation flag is raised. The acceptance window can be set either to 0, asking for equality in the comparison, or to 1,2 and 3 corresponding to 1,2 and 3 bit of difference.

4.6 Priority Selector and Preview Selector

This module selects one of the candidates according to some programmed information.

If the correlation was successful the priority selector chooses the correlated candidate and forwards its parameters to the further stages.

If the correlation fails the correlator creates an uncorrelated track following a preference list that includes the parent superlayer (Inner or Outer) and the quality bit (High or Low) of the two candidate tracks.

If no correlation is possible since there is no candidate in one Superlayer, the existing uncorrelated track is still accepted.

A preference selection can be activated to connect the trigger generated in the transverse view to the triggers generated from the BTIs in the longitudinal view. A programmable coincidence between the two views is foreseen to certify the uncorrelated triggers. In particular, since the noise generated from the BTI algorithm is concentrated in the LTRGs, this coincidence is requested by default for the LTRGs and it is optional for the HTRGs.

The First and the Second Track priority selectors treat the *best* inner candidate, the *best* outer candidate and the correlated candidate considering the trigger quality, the high level trigger mask (HTMSK), the low level trigger mask (LTMSK) and the Superlayer mask (SLMSK). The meaning of selection bits is given in the Table 1.

F(S)HTMSK	Single High quality triggers: (1) accepted only if coincident with Theta trigger (0) always accepted (default)
F(S)LTMSK	Single Low quality triggers: (1) always discarded (0) accepted only if coincident with Theta trigger (default)
F(S)SLMSK	Superlayer preference: (1) ? (0) ?

Table 1 – Track selection configuration bits.

Each priority selector sends only one candidate towards the output bus, and generates a three bits qualification code as shown in Table 2.

Description	***Symbol***	***Code***
HTRG on inner and outer layer (correlated)	HH	0
HTRG on inner/outer layer and LTRG on outer/inner layer (correlated)	HL	1
LTRG on inner and outer layer (correlated)	LL	2
HTRG on outer layer	H_o	3
HTRG on inner layer	H_i	4
LTRG on outer layer	L_o	5
LTRG on inner layer	L_i	6
Null track		7

Table 2 - Codes for output track quality identifier.

4.7 Recycling unused candidates

Two candidates are needed to fit a correlated track, one from the inner Superlayer and another from the outer one. If the correlated track does not satisfy the programmed acceptance value, only one of the track candidates selected to try the correlation is forwarded as the First Track choice. The other candidate must be reused for the Second Track calculations. This module allows to enable or disable this recycling task according to two programming bits: REUSEI and REUSEO with the meaning shown in

REUSEI	Inner candidate: (1) recycling enabled (0) no recycling
REUSEO	Outer candidate: (2) recycling enabled (0) no recycling

Table 3 – Recycling configuration bits.

Table 3.

4.8 Mixer

The two selected tracks are output on the same bus at consecutive bunch crossings. Therefore it is possible that a Second Track from the previous bunch crossing is computed at the same time of a First Track from the bunch crossing being considered. A

First Track choice has always priority on the output bus and therefore any First Track overlaps the Second Track choice from the previous bunch crossing. A flag is activated if an overlap occurs.

4.9 Coordinate converter and bending angle calculation

The internally calculated position and k-parameter are converted, to the chamber reference system: position is transformed to radial angle ϕ and k-parameter to bending angle ϕ_b as defined in Figure 4.

This task is performed passing track candidates k-parameter and position through two programmable look-up tables. The first look-up table is used for conversion of the position, coded in 9 bits, to the track radial angle ϕ, coded in 12 bits (11 bits plus the sign with 12 bits resolution). The second table performs the conversion from the k-parameter, coded in 10 bits to the angle with respect to the normal to the chamber ψ, coded in 10 bits (9 bits plus the sign with 9 bits resolution).

A further block performs the computation of the bending angle:

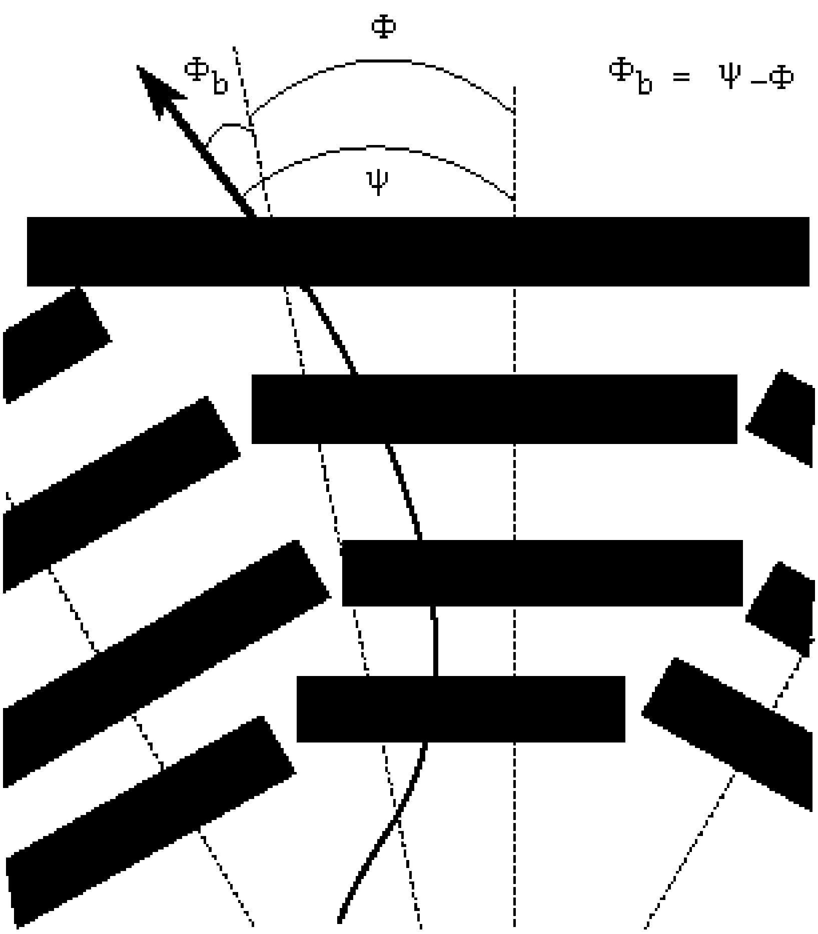

Figure 4 - Definition of the TRACO output parameters.

$$\phi_b = \phi - \psi$$

4.10 Quality filter

Some filtering functions are performed in this block to select the output value driven to the chamber server. These functions include the suppression of single low quality triggers (LTS) and a programmable acceptance window for the bending angle output value. With the LTS filter activated, double correlated and single low quality triggers are cancelled when they come within 4 clock cycles before a high quality trigger. The angular cut is applied to low quality triggers, either double correlated or single; when the absolute value of the bending angle is higher than a programmed value (KPRGCOM) the trigger is cancelled. The filters will be discussed in detail in paragraph 5.3.

4.11 Output Preview-Data Bus

TRACO Preview-Data bus provides one track at each clock cycle, with up to two tracks per bunch crossing at consecutive clock cycles.

The latency for the first track is three cycles, while the second one is output in the next cycle. In case two events generate triggers in two consecutive crossings and two tracks are detected correspondent to the first event, the second track of the first event is suppressed to allow the first track of the next event to be forwarded.

Selected tracks are output on a 9 bits bus, where 5 bits give the absolute value of the k-parameter, 1 bit the sign, and 3 bits the trigger quality: Correlated (SRVPCR), High/Low (SRVPHL) and Inner/Outer (SRVPIO). One bit is the first track strobe. The Preview bus is described in Table 4.

SRVPR<4:0>	Track k-parameter $1F is the default value for no trigger
SRVPR<5>	Sign of track k-parameter
SRVPCR	Flag for correlated track
SRVPHL	Flag for high/low (1/0) quality track
SRVPIO	Flag for Inner/Outer track (1) Outer trigger (0) Inner trigger
SRVPFS	Strobe for first track output (1) First track (0) Second track (if SRVPR <> $1F) or no trigger

Table 4 – TRACO Preview-Data bus.

4.12 Output Data Bus

TRACO Data Bus provides one track at each clock cycle, with up to two tracks per event at consecutive clock cycles.

The latency for the First Track is five cycles, while Second Tracks are output one cycle later. Similarly to the Preview-Data bus in case there are two events at contiguous bunch crossings, the second track from the first event is suppressed and the first track from the second event is forwarded.

The selected track is output on a bus, using 10 bits for the bending angle, 12 bits for the radial angle and three quality bits identifying track quality. One bit is the first track strobe. The Preview bus is described in Table 5.

SRVDT<26:15>	Radial angle (signed integer)
SRVDT<14:5>	Bending angle (signed integer)
SRVDT(4:2)	Track quality
SRVDT(1)	Overlap flag (1) track overlap
SRVDT(0)	Strobe for first track output (1) First track (0) Second track (if SRVPR <> $1F) or no trigger

Table 5 – TRACO Data bus.

5. TRACO Interfaces

The following paragraphs describe TRACO interfaces for control and monitoring.

5.1 Control Logic

This block contains a JTAG[1] interface and a bi-directional parallel interface. The JTAG port (tms, tck, tdi, tdo) can be used either to verify chip interconnections once it has been mounted on a PCB or to program internal registers. An additional capability of this interface is the monitoring of chip activity without interfering with the trigger function. This can be performed simply reading the snap registers connected to the input signals and to the output bus (see snap registers description in the next paragraph).

While both the parallel interface and the JTAG bus can be used to program the TRACO internal registers, only the parallel interface, much faster than the JTAG port, can be used to load the look-up tables needed for coordinate conversion. Using the dedicated preview bus the TSS has the possibility to access the internal registers of the connected TRACOs and downstream the Trigger Server Master (TSM) can access all chamber TSS.

[1] IEEE Std 1149.1-1990 "IEEE Standard Access Port and Boundary-Scan Architecture", May 21, 1990

Add	b5 (MSB)	b4	b3	b2	b1	b0 (LSB)
0	st43<5>	st43<4>	st43<3>	st43<2>	st43<1>	st43<0>
1	re43<1>	re43<0>	-	wen<9>	wen<8>	wen<7>
2	wen<6>	wen<5>	wen<4>	wen<3>	wen<2>	wen<1>
3	dead<5>	dead<4>	dead<3>	dead<2>	dead<1>	dead<0>
4	lh<5>	lh<4>	lh<3>	lh<2>	lh<1>	lh<0>
5	ll<5>	ll<4>	ll<3>	ll<2>	ll<1>	ll<0>
6	ch<5>	ch<4>	ch<3>	ch<2>	ch<1>	ch<0>
7	cl<5>	cl<4>	cl<3>	cl<2>	cl<1>	cl<0>
8	rh<5>	rh<4>	rh<3>	rh<2>	rh<1>	rh<0>
9	rl<5>	rl<4>	rl<3>	rl<2>	rl<1>	rl<0>
10	tston	test	ten	-	xon	ron
11	set<2>	set<1>	set<0>	lts<1>	lts<0>	-
12	ac1<1>	ac1<0>	ac2<1>	ac2<0>	acl<1>	acl<0>
13	ach<1>	ach<0>	-	-	-	-

Tab 4.1.1: Configuration register file.

5.2 Reset Logic

At power on all trigger chips can be put in a default state using the asynchronous reset line HRSTB. The synchronous reset (SYRSB) can be used to clear all internal registers with the exception of the configuration parameter register file.

An additional synchronous reset command (SNRSB) clears only the snap registers.

5.3 Internal register files

TRACO registers are grouped into 5 files of 8 bit words accessible using dedicated JTAG instruction addresses: configuration, test, snap, debug and boundary.

5.3.1 Configuration

This register file collects all the set up registers for the TRACO trigger operation and has to be programmed after a power-on reset (HRSTB low)

The section 7.0: Operating Instructions gives more information about the use of these parameters.

5.3.2 Test

This register file (Tab. 4.2.1) is mainly used to run self tests of the TRACO but can be used also to mask specific track patterns:

Address	b5	b4	b3	b2	b1	b0
14	-	-	-	-	ptms<31>	ptms<30>
15	ptms<29>	ptms<28>	ptms<27>	ptms<26>	ptms<25>	ptms<24>
16	ptms<23>	ptms<22>	ptms<21>	ptms<20>	ptms<19>	ptms<18>
17	ptms<17>	ptms<16>	ptms<15>	ptms<14>	ptms<13>	ptms<12>
18	ptms<11>	ptms<10>	ptms<9>	ptms<8>	ptms<7>	ptms<6>
19	ptms<5>	ptms<4>	ptms<3>	ptms<2>	ptms<1>	ptms<0>
20	tcen<11>	tcen<10>	tcen<9>	tcen<8>	tcen<7>	tcen<6>
21	tcen<5>	tcen<4>	tcen<3>	tcen<2>	tcen<1>	tcen<0>
22	wd1<5>	wd1<4>	wd1<3>	wd1<2>	wd1<1>	wd1<0>
23	wd2<5>	wd2<4>	wd2<3>	wd2<2>	wd2<1>	wd2<0>
24	wd3<5>	wd3<4>	wd3<3>	wd3<2>	wd3<1>	wd3<0>
25	wd4<5>	wd4<4>	wd4<3>	wd4<2>	wd4<1>	wd4<0>
26	wd5<5>	wd5<4>	wd5<3>	wd5<2>	wd5<1>	wd5<0>
27	wd6<5>	wd6<4>	wd6<3>	wd6<2>	wd6<1>	wd6<0>
28	wd7<5>	wd7<4>	wd7<3>	wd7<2>	wd7<1>	wd7<0>
29	wd8<5>	wd8<4>	wd8<3>	wd8<2>	wd8<1>	wd8<0>
30	wd9<5>	wd9<4>	wd9<3>	wd9<2>	wd9<1>	wd9<0>

Tab 4.2.1: Test register file.

The section 8.0: Test and Debug Features gives more information about track emulation procedure.

5.3.3 Snap

This register file (Tab. 4.3.1) is used for chip monitoring purposes:
The snap registers are cleared by a SNPRST signal and are written only once, after the first trigger occurrence.

IN	bit	description
w<9:1>		wire inputs
ferdb		Front-end read strobe
fewrb		Front-end write strobe
prgb		Parallel interface enable
strb		Parallel interface data strobe
rwb		Parallel interface read/write
trg<2:0>	2	Right trigger
	1	Center trigger
	0	Left trigger
hlb		Trigger quality
trgoeb		Trigger output enable
d<5:0>	5	Parallel interface data bus
ap<5:0>	5	Trigger angle/position bus
apoeb		Trigger ap bus enable

Tab 4.4.1: Boundary register file.

5.3.4 Boundary Scan

This register file (see Tab. 4.4.1) is accessible via JTAG and is used only for Trigger board connectivity tests.

Address	b5	b4	b3	b2	b1	b0
31	-	-	-	snw<9>	snw<8>	snw<7>
32	snw<6>	snw<5>	snw<4>	snw<3>	snw<2>	snw<1>
33	-	-	-	lqtr<2>	lqtr<1>	lqtr<0>
34	lpos<5>	lpos<4>	lpos<3>	lpos<2>	lpos<1>	lpos<0>
35	lang<5>	lang<4>	lang<3>	lang<2>	lang<1>	lang<0>
36	-	-	-	hqtr<2>	hqtr<1>	hqtr<0>
37	hpos<5>	hpos<4>	hpos<3>	hpos<2>	hpos<1>	hpos<0>
38	hang<5>	hang<4>	hang<3>	hang<2>	hang<1>	hang<0>
39	re23<1>	re23<0>	st23<4>	st23<3>	st23<2>	st23<1>
40	st23<0>	st<5>	st<4>	st<3>	st<2>	st<1>
41	st<0>	st2<6>	st2<5>	st2<4>	st2<3>	st2<2>
42	st2<1>	st2<0>	st3<6>	st3<5>	st3<4>	st3<3>
43	st3<2>	st3<1>	st3<0>	st4<7>	st4<6>	st4<5>
44	st4<4>	st4<3>	st4<2>	st4<1>	st4<0>	st5<7>
45	st5<6>	st5<5>	st5<4>	st5<3>	st5<2>	st5<1>
46	st5<0>	st7<7>	st7<6>	st7<5>	st7<4>	st7<3>
47	st7<2>	st7<1>	st7<0>	-	-	-

Tab 4.3.1: Snap register file

Instruction	Name	Description
0	EXTEST	Boundary scan test
1	-	-
2	SAMPLE	Chip boundary sampling
3	-	-
4	-	-
5	-	-
6	-	-
7	CONFIG	Configuration register file
8	TEST	Test register file
9	SNAP	Snap register file
10	DEBUG	Debugging register file
11	-	-
12	-	-
13	-	-
14	-	-
15	BYPASS	Chip bypassing

Tab 5.0.1: JTAG instruction set.

5.4 JTAG interface

The JTAG[7] port is available for interconnection testing and for TRACO registers programming. The implemented instructions are the mandatory Extest, Bypass and Sample, and the dedicated Config, Test, Snap and Debug as described in Tab. 5.0.1.

The first one (Extest) is used for PCB testing and in general for system interconnect verification. This function allows to write in all chip outputs a value and to verify that the same pattern can be received at the inputs of downstream connected devices.

The bypass instruction is used to skip a device in the JTAG chain.

Sample instruction allows to read TRACO periphery without interfering with chip operation.

Dedicated instructions are used to access Configuration, Test and Snap register files.

5.5 Parallel interface

The TRACO registers can be programmed very efficiently through a parallel interface. This port is controlled by three input lines: PRGB, STRB and R/W. The I/O data bus uses the same set of pins as the angle/position 6 bit trigger bus. As shown in Fig.6.0.1 a low level on PRGB turns on the interface and prevents any trigger data to be generated. The internal registers can be accessed randomly or sequentially.

After PRGB is pulled low the first input word is the address pointer and the second one is to read or write operation into the data register. If PRGB is kept low the address pointer is self-incremented and another datum can be read or written into the next register. When PRGB goes high the address pointer is cleared.

5.6 Operating instructions

TRACO operations start at power on with a hardware reset command, executed pulling low HRSTB. While CK and PHI are running, the synchronous reset command SYRSB can be used to clear the internal registers with the exception of the configuration register file. A dedicated synchronous reset (SNRSB) is available to clear only the snap register file and this operation does not interfere with the triggering function.

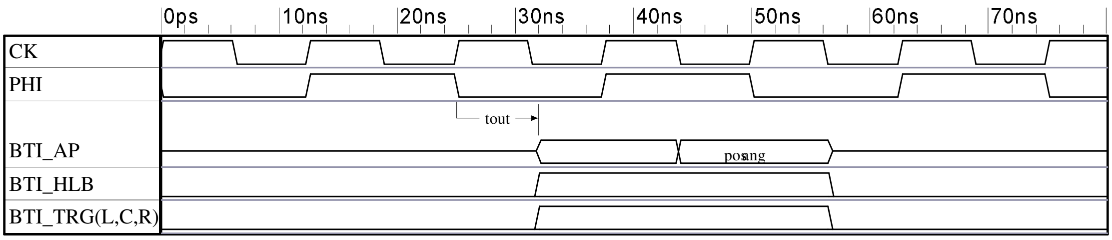

Fig. 7.0.1: BTI output timing.

CK and PHI are respectively the sampling clock and the output clock. The latched input signals coming from WIN are sampled at the rising edge of CK while trigger angle data are output at the falling edge of PHI (see the timing diagram of Fig.7.0.1).

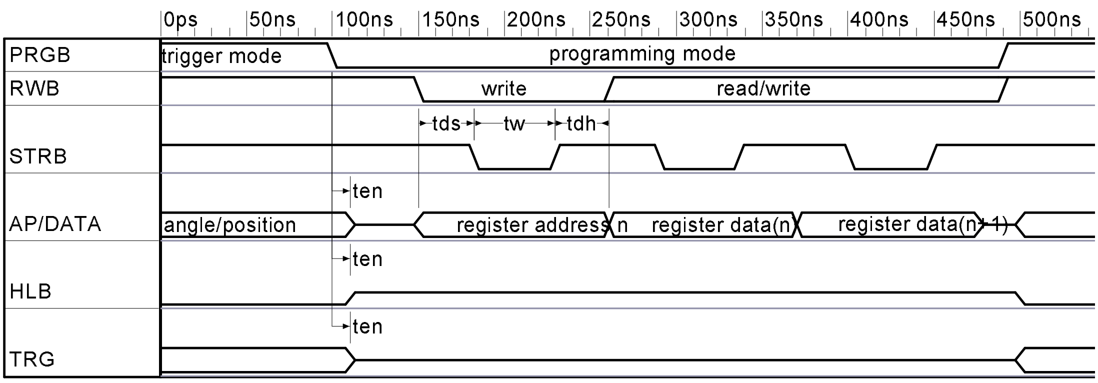

Fig. 6.0.1: Parallel Interface access timing.

The angle value is given first (during the low phase of PHI) and then the position is output during the high phase of PHI. It is foreseen that angle/position values are sampled by TRACOs on the rising/falling edge of PHI respectively, while trigger strobes and quality bit are sampled on the rising edge of PHI. In order to enable the trigger data bus, PRGB must be high.

The BTI output is meaningless for the first 20 PHI cycles after an hardware reset (HWRST low).

The BTI trigger set-up is described in the next four steps.

5.7 Trigger filtering parameters

Each input wire has a mask bit in the WEN register: noisy channels can be individually disabled by setting high the correspondent mask bit.

The trigger output can be filtered both in time and angle. LH and LL are the high and low angle thresholds for the Left Trigger (LTRG) (confonde!!!!)strobe defining the left region acceptance size. The registers CH, CL and RH, RL have the same meaning respectively for Central Trigger (CTRG) and Right Trigger (RTRG).

The LTS algorithm is turned on when LTS is not zero according to the following table:

LTS<1:0>	Low quality Trigger Suppression
00	none
01	after a high quality trigger for SET<2:0> PHI cycles
10	before a high quality trigger for 1 PHI cycle
11	after and before a high quality trigger (01 and 10)

Tab. 7.2.1: LTS algorithm setup.

Flags XON and RON play an important role in the trigger efficiency to noise ratio. The first one, when set high, turns on all low quality triggers of tracks passing from the same side of the wires; this enhances slightly the trigger efficiency at high angle but increases the trigger noise. RON, when set high, turns on the redundant track patterns, that is the patterns that should be covered by the neighbouring BTIs. This can be helpful if the BTI is the last one of the Superlayer or the neighboring BTI is disabled, or mulfunctioning.

5.8 Test and debug features

The BTI chip has a built in self test logic aiming to minimize the vectors for chip validation. The validation mode is activated by flags VAL and TSTON, as explained in detail in Appendix E.

Snap registers, connected to input wire signals and output trigger data are provided for online trigger system debugging. The input wire snap flip-flops are set if a signal has been received by the BTI after the last reset (SNRSB). The output trigger data snap registers keep the full trigger information: LTRG, CTRG, RTRG, H/L, ANG<5:0> and POS<5:0> either for the first low quality trigger occurred or the first high quality trigger generated after the last reset. After a SNRSB reset command, the JTAG interface can be used to shift out the snap register data allowing to monitor the trigger activity without any interference.

Another testing facility is the possibility to disconnect by software the BTI from the chamber and to use internal programmable delays as drift cell emulators. Setting high the TEN flag makes the wire inputs WIN to be inactive. The internal registers WD1<5:0> to WD9<5:0> are the starting values of drift time counters. Once these registers are programmed to be equal to the drift times (in 12.5ns steps) associated to a test track, setting high the TSTON flag makes the drift counters to start counting down, simulating the track signal generation. If WDn<5:0> is set to zero the relative wire doesn't give any signal. This capability to simulate real tracks can be used on the field to test the trigger chain in special situations.

Appendix A: TRACO Technical Specification

. Operating voltage 3.3V ± 0.3V
. TTL/CMOS compatible inputs
. Operating speed 40MHz (80MHz input sampling of BTI busses)
. Low power 0.5µm CMOS process
. JTAG interface
. Parallel interface
. Emulation and monitoring features
. Short lead QFP 240 pin package

SQFP240 pinout

Pin	Name	Type	Pin	Name	Type
1	Vdd	Core	38	Srvpcr	Out 3-State + pullup
2	VddAC	Periphery AC	39	Srvpfs	Out 3-State + pullup
6	Bti13dt0	Input + pulldown	40	Srvphl	I/O + pullup
7	Bti13dt1	Input + pulldown	41	Srvpio	I/O + pullup
8	Bti13dt2	Input + pulldown	42	Srvpr0	I/O + pullup
9	Bti13dt3	Input + pulldown	43	Srvpr1	I/O + pullup
10	Bti13dt4	Input + pulldown	44	Srvpr2	I/O + pullup
11	Bti13dt5	Input + pulldown	45	Srvpr3	I/O + pullup
12	Bti13trg	Input + pulldown	46	Srvpr4	I/O + pullup
13	Bti13hlb	Input + pulldown	47	Srvpr5	I/O + pullup
14	Bti14dt0	Input + pulldown	48	Tck	Input Schmitt + pulldown
15	Bti14dt1	Input + pulldown	49	Tms	Input Schmitt + pullup
16	Bti14dt2	Input + pulldown	50	Tdi	Input Schmitt + pullup
17	Bti14dt3	Input + pulldown	51	Tdo	Out 3-State + pullup
18	Bti14dt4	Input + pulldown	52	Bist_test	Input Schmitt + pulldown
19	Bti14dt5	Input + pulldown	53	Seqrst	Input Schmitt + pulldown
20	Bti14trg	Input + pulldown	54	Seqtst	Input Schmitt + pulldown
21	Bti14hlb	Input + pulldown	55	Seqadv	Input Schmitt + pulldown
22	Bti15dt0	Input + pulldown	59	VssAC	Periphery AC
23	Bti15dt1	Input + pulldown	60	VssDC	Periphery DC
24	Bti15dt2	Input + pulldown	61	Vss	Core
25	Bti15dt3	Input + pulldown	62	VssAC	Periphery AC
26	Bti15dt4	Input + pulldown	63	VddAC	Periphery AC
27	Bti15dt5	Input + pulldown	64	Bti4hlb	I/O + pulldown
28	Bti15trg	Input + pulldown	65	Bti4trg	Input + pulldown
29	Bti15hlb	Input + pulldown	66	Bti4dt5	I/O + pulldown
30	Bti16dt0	Input + pulldown	67	Bti4dt4	I/O + pulldown
31	Bti16dt1	Input + pulldown	68	Bti4dt3	I/O + pulldown
32	Bti16dt2	Input + pulldown	69	Bti4dt2	I/O + pulldown
33	Bti16dt3	Input + pulldown	70	Bti4dt1	I/O + pulldown
34	Bti16dt4	Input + pulldown	71	Bti4dt0	I/O + pulldown
35	Bti16dt5	Input + pulldown	72	Bti3hlb	I/O + pulldown
36	Bti16trg	Input + pulldown	73	Bti3trg	Input + pulldown
37	Bti16hlb	Input + pulldown	74	Bti3dt5	I/O + pulldown

Pin	Name	Type	Pin	Name	Type
75	Bti3dt4	I/O + pulldown	109	Srvdt1	Output 3-State + pullup
76	Bti3dt3	I/O + pulldown	110	Srvdt2	Output 3-State + pullup
77	Bti3dt2	I/O + pulldown	111	Srvdt3	Output 3-State + pullup
78	Bti3dt1	I/O + pulldown	112	Srvdt4	Output 3-State + pullup
79	Bti3dt0	I/O + pulldown	113	Srvdt5	Output 3-State + pullup
80	Bti2hlb	I/O + pulldown	114	Srvdt6	Output 3-State + pullup
81	Bti2trg	Input + pulldown	115	Srvdt7	Output 3-State + pullup
82	VssAC	Periphery AC	116	Srvdt8	Output 3-State + pullup
83	VddAC	Periphery AC	117	Srvdt9	Output 3-State + pullup
84	Bti2dt5	I/O + pulldown	118	Srvdt10	Output 3-State + pullup
85	Bti2dt4	I/O + pulldown	119	VddAC	Periphery AC
86	Bti2dt3	I/O + pulldown	120	VddDC	Periphery DC
87	Bti2dt2	I/O + pulldown	122	Vdd	Core
88	Bti2dt1	I/O + pulldown	123	VddAC	Periphery AC
89	Bti2dt0	I/O + pulldown	127	VssAC	Periphery AC
90	Bti1hlb	I/O + pulldown	128	Theta	Input Schmitt + pulldown
91	Bti1trg	Input + pulldown	129	Orhl	Input Schmitt + pulldown
92	Bti1dt5	I/O + pulldown	130	Olhl	Input Schmitt + pulldown
93	Bti1dt4	I/O + pulldown	131	Irhl	Input Schmitt + pulldown
94	Bti1dt3	I/O + pulldown	132	Ilhl	Input Schmitt + pulldown
95	Bti1dt2	I/O + pulldown	133	Snprstb	Input Schmitt + pullup
96	Bti1dt1	I/O + pulldown	134	Sresetb	Input Schmitt + pullup
97	Bti1dt0	I/O + pulldown	135	Resetb	Input Schmitt + pullup
98	Vss	Core	136	Prgb	Input Schmitt + pulldown
99	Vdd	Core	137	Select	Input Schmitt + pulldown
100	VddDC	Periphery DC	138	Postsel	Input Schmitt + pulldown
101	Vss	Core	139	Srvdt11	Output 3-State + pullup
102	VssDC	Periphery DC	140	Srvdt12	Output 3-State + pullup
103	Vss	Core	141	Srvdt13	Output 3-State + pullup
104	VddDC	Periphery DC	142	Srvdt14	Output 3-State + pullup
105	Clock	Input Schmitt + pulldown	143	VddAC	Periphery AC
106	VssDC	Periphery DC	144	VssAC	Periphery AC
107	Btistrb	Out 3-State + pullup	145	Srvdt15	Output 3-State + pullup
108	Srvdt0	Output 3-State + pullup	146	Srvdt16	Output 3-State + pullup

Pin	Name	Type	Pin	Name	Type
147	Srvdt17	Output 3-State + pullup	195	Bti8dt1	Input + pulldown
148	Srvdt18	Output 3-State + pullup	196	Bti8dt2	Input + pulldown
149	Srvdt19	Output 3-State + pullup	197	Bti8dt3	Input + pulldown
150	Srvdt20	Output 3-State + pullup	198	Bti8dt4	Input + pulldown
151	Srvdt21	Output 3-State + pullup	199	Bti8dt5	Input + pulldown
152	Srvdt22	Output 3-State + pullup	200	Bti8trg	Input + pulldown
153	VddAC	Periphery AC	201	Bti8hlb	Input + pulldown
154	VssAC	Periphery AC	202	Bti9dt0	Input + pulldown
155	Srvdt23	Output 3-State + pullup	203	Bti9dt1	Input + pulldown
156	Srvdt24	Output 3-State + pullup	204	Bti9dt2	Input + pulldown
157	Srvdt25	Output 3-State + pullup	205	Bti9dt3	Input + pulldown
158	Srvdt26	Output 3-State + pullup	206	Vss	Core
159	Vss	Core	207	Vdd	Core
160	Vdd	Core	208	Bti9dt4	I/O + pulldown
161	Bti5dt0	Input + pulldown	209	Bti9dt5	I/O + pulldown
162	Bti5dt1	Input + pulldown	210	Bti9trg	Input + pulldown
163	Bti5dt2	Input + pulldown	211	Bti9hlb	I/O + pulldown
164	Bti5dt3	Input + pulldown	212	Bti10dt0	I/O + pulldown
165	Bti5dt4	Input + pulldown	213	Bti10dt1	I/O + pulldown
166	Bti5dt5	Input + pulldown	214	Bti10dt2	I/O + pulldown
167	Bti5trg	Input + pulldown	215	Bti10dt3	I/O + pulldown
168	Bti5hlb	Input + pulldown	216	Bti10dt4	I/O + pulldown
169	Bti6dt0	Input + pulldown	217	Bti10dt5	I/O + pulldown
170	Bti6dt1	Input + pulldown	218	Bti10trg	Input + pulldown
171	Bti6dt2	Input + pulldown	219	Bti10hlb	I/O + pulldown
172	Bti6dt3	Input + pulldown	220	Bti11dt0	I/O + pulldown
173	Bti6dt4	Input + pulldown	221	Bti11dt1	I/O + pulldown
174	Bti6dt5	Input + pulldown	222	Bti11dt2	I/O + pulldown
175	Bti6trg	Input + pulldown	223	Bti11dt3	I/O + pulldown
176	Bti6hlb	Input + pulldown	224	Bti11dt4	I/O + pulldown
177	Bti7dt0	Input + pulldown	225	Bti11dt5	I/O + pulldown
178	Bti7dt1	Input + pulldown	226	Bti11trg	Input + pulldown
179	VssAC	Periphery AC	227	Bti11hlb	I/O + pulldown
180	VssDC	Periphery DC	228	Bti12dt0	I/O + pulldown
184	Vss	Core	229	Bti12dt1	I/O + pulldown
185	VssAC	Periphery AC	230	Bti12dt2	I/O + pulldown
187	VddAC	Periphery AC	231	Bti12dt3	I/O + pulldown
188	Bti7dt2	Input + pulldown	232	Bti12dt4	I/O + pulldown
189	Bti7dt3	Input + pulldown	233	Bti12dt5	I/O + pulldown
190	Bti7dt4	Input + pulldown	234	Bti12trg	Input + pulldown
191	Bti7dt5	Input + pulldown	235	Bti12hlb	I/O + pulldown
192	Bti7trg	Input + pulldown	236	VssAC	Periphery AC
193	Bti7hlb	Input + pulldown	239	VddAC	Periphery AC
194	Bti8dt0	Input + pulldown	240	VddDC	Periphery DC

Absolute maximum ratings

Parameter	Min	Max	Unit	Conditions
DC supply voltage	-0.3	4.6	V	
DC input diode current	-10	10	mA	
DC output diode current	-10	10	mA	
Time of otputs shorted		5	s	
Storage temperature	-65	150	°C	
Ambient free air temperature range	-40	85	°C	Industrial

Recommended operating conditions

Electrical characteristics				
Parameter	Min	Typ	Max	Conditions
DC supply voltage	3.0V	3.3V	3.6V	
Low level input voltage	-0.3V		0.3*Vdd	
High level input voltage	0.7*VDD		Vdd+0.3V	
Low level output v.ge			Vss+0.1V	2.7V IOL=0.3mA CMOS
High level output v.ge	Vdd-0.1V			2.7V IOL=0.3mA CMOS
Low level output v.ge			0.4V	2.7V IOL=2 to 8 mA TTL
High level output v.ge	2.4V			2.7V IOL=2 to 8mA TTL
Pullups and pulldowns				
Pullup current	-77µA		-300µA	@0V worst case
Pulldown current	79µA		396µA	@3.3V worst case
AC output characteristics [2]				
Bti_dt_, Bti_hlb, Tdo	0.168	0.095	0.052	ns/pF rise time
	0.188	0.106	0.058	ns/pF fall time
		2mA		AC Drive current
		2mA		DC Drive current
Srvp*, Btistrb	0.085	0.048	0.026	ns/pF rise time
	0.094	0.053	0.029	ns/pF fall time
		4mA		AC Drive current
		2mA		DC Drive current
Srvdt*	0.058	0.033	0.018	ns/pF rise time
	0.064	0.036	0.020	ns/pF fall time
		6mA		AC Drive current
		2mA		DC Drive current
AC input characteristics				
Input rise time			10ns	CMOS and TTL inputs
Input rise time			No limit	Schmitt inputs
Schmitt input threshold	1.39V	1.66V	1.8V	VT+
"	0.85V	1.05V	1.16V	VT-
Schmitt input hysteresis	0.48V	0.62V	0.66V	

[1] Worst case temperature, voltage and process corners.

[2] Unless otherwise specified VDD=3.3V, T=25°C, typical process, input slope = 1ns.

Package characteristics

SQFP240	Thermal resistance	35°C/W
	Lead resistance	63 - 80 mΩ
	Self inductance	7.7 – 11 nH
	Mutual inductance	5.0 – 7.5 nH
	Bulk capacitance	1.5 – 2.3 pF
	Mutual capacitance	0.7 – 1.0 pF

Common dimensions (mm) for pin count from 64 to 208:

Common dimensions (mm) for pin count from 240 to 304:

Dimensions depending from lead count:

Pin Count	A Max	A1 Min	A1 Max	A2 Min	A2 Nom	A2 Max	b Min	b Max	b1 Min	b1 Nom	b1 Max
44	2.70	0.25	0.50	1.80	2.00	2.20	0.29	0.45	0.29	0.35	0.41
[illegible]											
256	4.10	0.25	0.50	3.20	3.40	3.60	0.13	0.23	0.13	0.16	0.19
304 ♦♦	4.50	0.25	0.50	3.60	3.80	4.00	0.17	0.27	0.17	0.20	0.23

Pin Count	D BSC	D1 BSC	E BSC	E1 BSC	e BSC	ddd
44	13.20	10.00	13.20	10.00	0.8	0.2
[illegible]						
256	30.60	28.00	30.60	28.00	0.40	0.10
304 ♦♦	42.60	40.00	42.60	40.00	0.50	0.10

Note:

♦ these packages are rectangular

♦♦ Pin number: 6, 18, 30, 42, 54, 66, 82, 94, 106, 118, 130, 142, 158, 170, 182, 194, 206, 218, 234, 246, 258, 270, 282, 294 must be connected to GND. Pin number: 7, 19, 31, 43, 55, 67, 83, 95, 107, 119, 131, 143, 159, 171, 183, 195, 207, 219, 235, 247, 259, 271, 283, 295 are interconnected to VCC.

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Short Lead Quad Flat Pack (SQFP)
& Enhanced Thermal Dissipation Quad Flat Pack (HQFP)
Foot Print 3.2 mm

Common dimensions (mm) for pin count from 64 to 208:

Symbol	Min	Nom	Max
c	0.11		0.23
c1	0.11	0.15	0.19
L	0.65	0.88	1.03
L1	1.60 REF.		
R2	0.13		0.3
R1	0.13		
S	0.4		
Tolerances of form and position			
aaa		0.25	
ccc			0.1

Common dimensions (mm) for pin count from 240 to 304:

Symbol	Min	Nom	Max
c	0.09		0.20
c1	0.09		0.16
L	0.45	0.60	0.75
L1	1.30 REF.		
R2	0.08		0.25
R1	0.08		
S	0.20		
Tolerances of form and position			
aaa		0.20	
ccc			0.1

Dimensions depending from lead count:

Pin	A	A1		A2			b		b1		
Count	Max	Min	Max	Min	Nom	Max	Min	Max	Min	Nom	Max
44	2.70	0.25	0.50	1.80	2.00	2.20	0.29	0.45	0.29	0.35	0.41
52	2.45	0.00	0.25	1.80	2.00	2.20	0.34	0.50	0.34	0.40	0.46
64 ♦	3.4	0.25	0.50	2.55	2.8	3.05	0.35	0.5	0.35	0.4	0.45
80 ♦	3.4	0.25	0.50	2.55	2.8	3.05	0.3	0.45	0.3	0.35	0.4
100 ♦	3.4	0.25	0.50	2.55	2.8	3.05	0.22	0.38	0.22	0.3	0.33
120	4.10	0.25	0.50	3.20	3.40	3.60	0.29	0.45	0.29	0.35	0.41
128	4.10	0.25	0.50	3.20	3.40	3.60	0.29	0.45	0.29	0.35	0.41
144	4.10	0.25	0.50	3.20	3.40	3.60	0.29	0.45	0.29	0.35	0.41
160	4.10	0.25	0.50	3.20	3.40	3.60	0.29	0.45	0.29	0.35	0.41
208	4.10	0.25	0.50	3.20	3.40	3.60	0.17	0.27	0.17	0.20	0.23
240	4.10	0.25	0.50	3.20	3.40	3.60	0.17	0.27	0.17	0.20	0.23
256	4.10	0.25	0.50	3.20	3.40	3.60	0.13	0.23	0.13	0.16	0.19
304 ♦♦	4.50	0.25	0.50	3.60	3.80	4.00	0.17	0.27	0.17	0.20	0.23

Pin Count	D BSC	D1 BSC	E BSC	E1 BSC	e BSC	ddd
44	13.20	10.00	13.20	10.00	0.8	0.2
52	13.20	10.00	13.20	10.00	0.65	0.13
64 ♦	23.20	20.00	17.20	14.00	1.0	0.2
80 ♦	23.20	20.00	17.20	14.00	0.80	0.2
100 ♦	23.20	20.00	17.20	14.00	0.65	0.12
120	31.20	28.00	31.20	28.00	0.80	0.2
128	31.20	28.00	31.20	28.00	0.80	0.2
144	31.20	28.00	31.20	28.00	0.65	0.12
160	31.20	28.00	31.20	28.00	0.65	0.12
208	31.20	28.00	31.20	28.00	0.50	0.10
240	34.60	32.00	34.60	32.00	0.50	0.10
256	30.60	28.00	30.60	28.00	0.40	0.10
304 ♦♦	42.60	40.00	42.60	40.00	0.50	0.10

Note:

♦ these packages are rectangular

♦♦ Pin number: 6, 18, 30, 42, 54, 66, 82, 94, 106, 118, 130, 142, 158, 170, 182, 194, 206, 218, 234, 246, 258, 270, 282, 294 must be connected to GND.
Pin number: 7, 19, 31, 43, 55, 67, 83, 95, 107, 119, 131, 143, 159, 171, 183, 195, 207, 219, 235, 247, 259, 271, 283, 295 are interconnected to VCC.

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