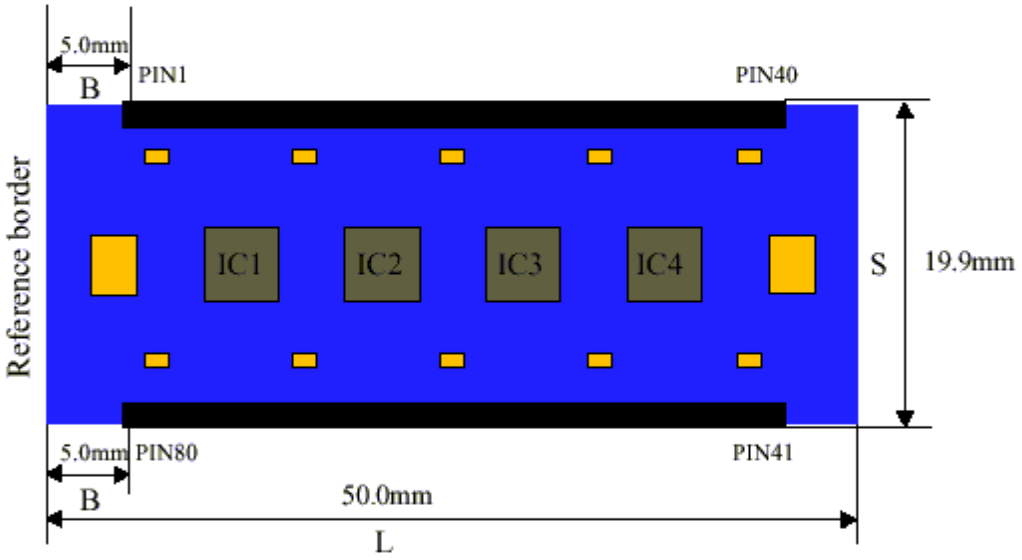
BTIM Technical Specification

Technical requirements:

1. Multi-chip Module description

The BTIM is a multi-chip module (see drawing), consisting of four ASICs and some passive components lodged on a ceramic substrate (not beryllia).



Bottom view

Module dimensions and tolerances are:

L : 50.0 [+0.0, -0.2] mm substrate length

W: 19.5 [± 0.1] mm substrate width

T : 0.6 [± 0.05] mm substrate thickness

H : 3.3 [± 0.2] mm height including terminations

S : 19.0 [+0.0, -0.3] mm width

B: 5.0mm [± 0.1] mm distance between borders of pins 1 and 80 from module reference side.

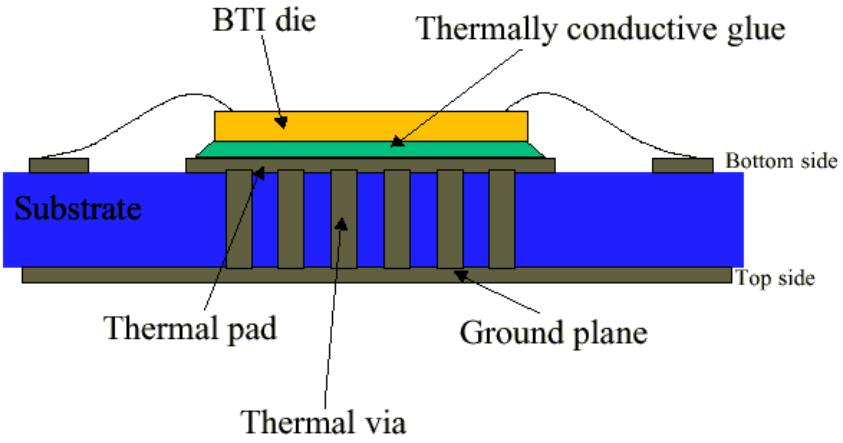
Module components are:

- 8 capacitors SMT 0.01uF X7R
- 4 dies BTI96 (KGD provided by INFN in waffle pack)
- 2 capacitors SMT (case EIA-norm 3528) 4.7uF SIEMENS model B45196-E

- Terminations: DIL 80 pin SMT 0.040” pitch from NAS Interplex model 22AA. Particular care is required in the centering of pins with respect to substrate borders.

The supplier has responsibility to select BTIM components considering the reliability requirements of the final product.

All components are placed on the bottom side. Dies are glued with good thermal conduction to the substrate and wire bonded with 62 wires each. Minimum pad pitch is about 100µm and passivation openings are 85µm x 85µm. A ground plane must be provided on the substrate top side with thermal vias for optimal BTI dies cooling (see drawing). BTI backside could be electrically connected to ground. Dies gooping is necessary for mechanical protection from MCM handling.



Power supply (3.3V) is applied through 2 pins for VDD and 4 pins for VSS.
The operating environment is defined in the following table:

environmental specifications	min	typ	max	unit	note
Operating temperature	0	40	70	°C	
Storage temperature	-20	20	70	°C	
Operating humidity			60	%RH	13°C dew point

Power consumption is less than 1W at 80MHz operating frequency. Four pins are used for clock distribution: two PHI (40MHz) and two CK (80MHz) lines, with a loading of two BTIs for each line. The number of nets on the substrate is 79 including VDD and VSS.

Module pinout is fixed and is provided in Appendix A. A copy of ATMEL bonding rules is given in Appendix B. The pad placement file of BTI can be found in Appendix C. BTIM schematic is provided in Appendix D.

2. Test and quality assurance

The modules must be delivered fully tested. Static vectors will be used to verify module connectivity, while dynamic vectors, to be generated at 40MHz, will be used for functional tests at full speed. Test vector sets, initially provided by the purchaser, could be modified after the prototype production in order to achieve the best defect screening capability.
Module reliability will be evaluated taking MIL-PRF-38534 procedures as a guideline (MIL standards are available at the STINET web page). Defective devices screening and production quality are achieved following the test flow given in the following table.

Test or inspection	**MIL-STD-883 Method**	**Requirement**
Internal visual	2017	100%
Preseal burn-in	1030	Qualification sample
Electrical test @ 25°C	Specified " Electrical Test"	Qualification sample
Nondestrutive bond pull	2023	Qualification sample
Seal	1014	100%
Stabilization bake	1008: 150°C 1 hour	100%
Temperature cycling	1010 condition C	100%
Electrical test @ 25°C	Specified " Electrical Test"	100%
Burn-in	1015	100%
Electrical test @ 25°C	Specified " Electrical Test"	100%
External visual	2009	100%
Steady-state life test	1005: 1000 hours at +125°C or equivalent	Qualification sample
Electrical test @ 25°C	Specified " Electrical Test"	Qualification sample
Internal water vapor content	1018 at +100°C	Qualification sample(*)
ESD	3015	Qualification sample (*)
Electrical test @ b25 deg.	Specified " Electrical Test"	Qualification sample (*)
(*) For prototype validation only		

Production screening flow should include the following steps:

- Internal visual method-2017
- Seal method-1014
- Stabilization bake method-1008: 150°C 1 hour
- Temperature cycling method-1010 condition C

- Electrical test @ 25°C Specified “Electrical Test”
- Burn-in method-1015
- Electrical test @ 25°C Specified “Electrical Test”
- External visual method-2009

An electrical test is required to verify connectivity and bonding integrity after module assembly; static vectors will use JTAG circuitry integrated in the BTIs to perform this test. A functional test is required to verify the module at full speed; dynamic vectors must be generated at 40MHz while module output must be acquired at 80MHz. The functional test can be repeated after any production phase (assembly, encapsulation, baking, thermal cycling, burn-in) to identify potential problems in the manufacturing procedure. The supplier will be provided with stimuli vector files for static and dynamic tests and MCM sockets in adequate quantity. Socket drawings can be found in Appendix E. The combination of thermal cycling and burn-in tests will be optimized after the prototyping and pre-production phases for best screening efficiency. Static life tests (according to MIL-STD-883 method 1005.8 and MIL-PRF-38534) will be performed on production samples to verify the screening procedure.

A qualification sample of 5 devices will be selected from each lot in order to verify quality uniformity of production. Qulaification sample tests should include the following steps:

- Internal visual method-2017
- Preseal burn-in method-1030
- Electrical test @ 25°C Specified “Electrical Test”
- Nondestrutive bond pull method-2023
- Seal method-1014
- Stabilization bake method-1008: 150°C 1 hour
- Temperature cycling method-1010 condition C
- Electrical test @ 25°C Specified “Electrical Test”
- Burn-in method-1015
- Electrical test @ 25°C Specified “Electrical Test”
- External visual method-2009
- Steady-state life test method-1005: 1000 hours at +125°C or eq.
- Electrical test @ 25°C Specified “Electrical Test”

The following additional tests will be required on prototype qualification lots:

- Internal water vapor content method-1018 at +100°C
- ESD method-3015
- Electrical test @ b25 deg. Specified “Electrical Test”

Lots failing qualification tests may be reworked and/or retested but they will be kept separate from new lots and will be clearly identified as reworked/retested lots. A second qualification test using double the initial sample size with zero failures allowed is permitted in the following cases:

- failure analysis is performed to determine the mechanism of failure for each failed device from the prior sample and it is determined that failure is due to a defect that can be effectively removed by rescreening the entire lot,
- the defect is random type which do not reflect poor basic device design or poor basic processing procedures.

In all lots where analysis of the failed devices indicates that the failure mechanism is due to poor basic processing procedures, a basic design fault, or not screenable defects, the lot will not be retested and will be discarded.
In case of defective lots CERN/CMS has the right to decide on the proper corrective and preventive actions to be taken.
During production screening, all multiple device failures must be analyzed to determine root cause. Multiple device failures with the same root cause (three or more depending on lot size) will be considered a "failure pattern". The lot will be stopped and placed on hold only if a pattern failure is established.
In all cases, lots with device failures that do not exceed the PDA are acceptable and do not require pattern failure analysis. The number of device failures with the same root cause that establish a failure pattern are based on lot size, as follows:

Lot size (x)	Number of failures establishing a pattern
x £ 20	3
21£ x £ 40	4
40 < x £ 100	5
100 < x £ 300	6
300 < x £ 500	11
500 < x	16

If the internal water vapor content exceeds 5000 ppmv (parts per million volume) at +100°C on more than one device, 5 additional screened samples will be subjected to 20 cycles of MIL-STD-883, method 1010 temperature cycling, condition C. Following temperature cycling the samples will be retested for internal water vapor content. Other gas species present in quantities greater than 100 ppmv (0.01 percent) must be reported. Two devices minimum will be tested to assure the post seal bond strength requirements of MIL-STD-883, method 2011. The bond strength test will be performed on a sample size (accept number) of 15(0) bond wires for each wirebond process (including each rework method outlined in C.7.6.4.10.1

as a separate process) and material (wire metallization) present in the device. Each 15 piece sample of wires will contain an even distribution of all wire sizes that can be qualified by that sample. No failures will be allowed. Additional devices will be added, if necessary, to meet the required wire sample size. The test wires will be predesignated.
Additional tests and inspections may be required where experience indicates concern for specific quality characteristics.

Option A: The supplier may provide its proposal of production screening procedure, clearly indicating possible advantages.

The contractor shall maintain a record of the detected failures in terms of number of defective MCM devices and when the failure has been detected with references to involved component lots.
The contractor is responsible for ensuring that all the necessary precautions are taken to maintain the specific manufacturing processes in use, under control during the MCM production, in order to assure repeatability and production homogeneity.
The company must inform the technical responsible, and receive his authorization prior to making any change(s) to the product and/or its sub-components. Modified products will be subject to re-qualification by the CERN/CMS technical staff.

3. Delivery schedule

The supplier shall provide a prototype production during 2001 of about 500 modules, tested against the previously described specifications. Mass production will be authorized by the purchaser only after approval of the prototype production.
CERN/CMS reserves the right to terminate the contract in case of failure of the prototypes or the pre-production to meet these technical requirements, without any compensation being due to the contractor with regard to such termination.
The production should be compatible with a delivery plan distributed over 2 years (2002 and 2003), with a roughly even distribution of deliveries.
The preferred delivery schedule is:
Prototype production: 50 pieces by September 2001.
Pre-series production: 450 pieces by December 2001.
Series production: 4 lots of 3000 pieces each, delivered by March 2002, September 2002, March 2003 and September 2003

In the quotation the following costs must be indicated:

- Non recurrent engineering
- Passive and active components
- Prototype production of 1500 pieces
- BTIM assembly
- Test and burn-in of modules
- Production lot of 3000 tested pieces

Option B: The supplier may propose and quote an alternative delivery schedule, clearly indicating possible cost reductions.

Persons in Charge

Commercial Contact: Dante Gregorio
CERN, SPL Division
CH1211 Geneva 23
Tel: + 41 22 767 6335
Fax: + 41 22 767 7530
E-mail: Dante.Gregorio@cern.ch

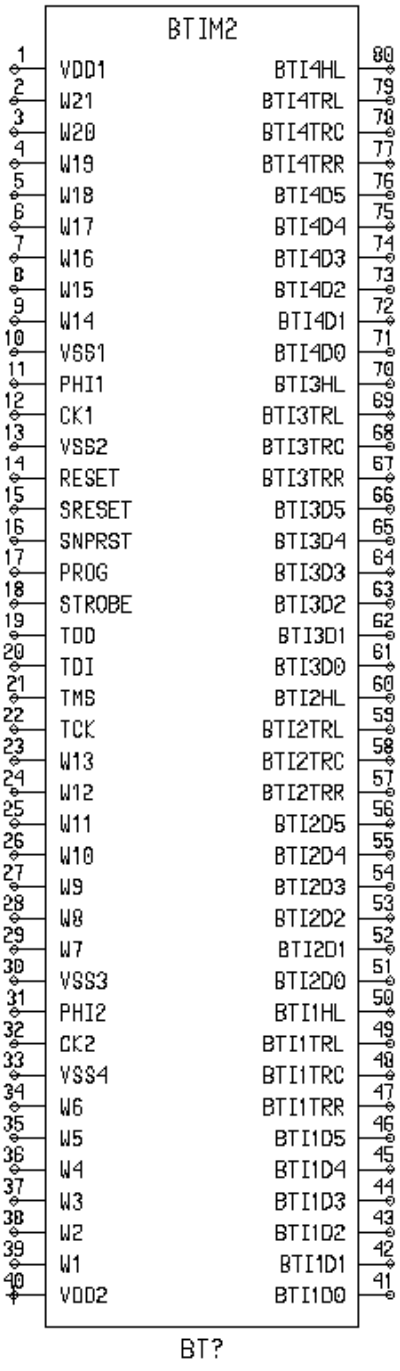
In case of absence: Paula Ribeiro
CERN, SPL Division
CH1211 Geneva 23
Tel: + 41 22 767 6991
Fax: + 41 22 767 7530
E-mail: Paula.Ribeiro@cern.ch

Technical Contact R. Martinelli
Tel: + 39 49 8277206
Fax: + 39 49 8277102
E-mail: roberto.martinelli@pd.infn.it

In case of absence: U. Dosselli
Tel: + 39 49 8277109
Fax: + 39 49 8756233
E-mail: umberto.dosselli@pd.infn.it

Appendix A

BTIM pinout



Appendix B

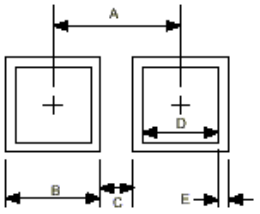
ATMEL boding rules

ASSEMBLY RULES

These assembly rules are applicable to all devices assembled with gold and aluminum bonding in plastic or ceramic packages at our subcontractor's sites.

1. Bond pad design rules

The following figure and table give the dimensions for the pad depending on the pad pitch.



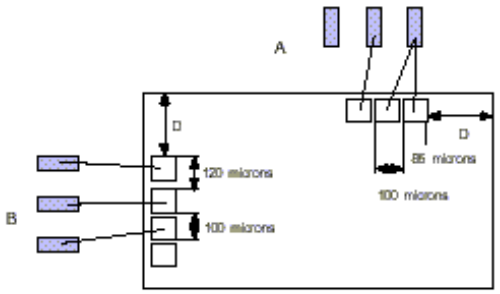
A: Bond pad pitch
B: Bond pad size
C: Pad to pad clearance
D: Bond pad opening
E: Glassivation area on pad

A (µm)	B (µm)	C (µm)	D (µm)	E (µm)
90	82	8	75	3.5
80	70	10	65	2.5
75	70	5	65	2.5

The SOIC and PDIP will accept a pad pitch lof 75 µm end Q4'98.

The minimum pitch is **90 µm** for all product assembled in volume in ceramic packages.

2 Corner rules



D: Bond pad edge to die edge

The distance D must be between 254 µm and 381 µm.

The rules described in the following chapter are applicable for the pad pitch less than 120 µm in the four corners. These rules must be used 8 times at each end of row. These rules are needed to avoid a short circuit in the corner during the molding.

Two possible designs for a corner cell are described in the previous figure.

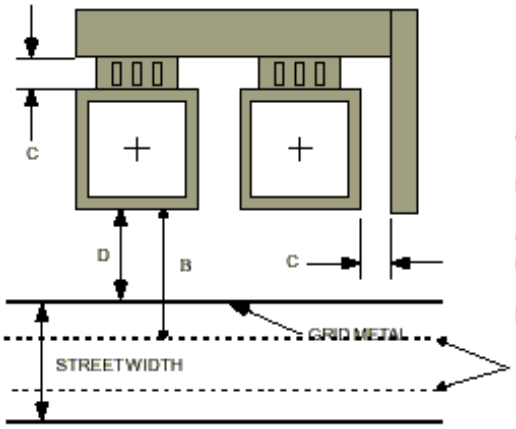
Case A:

The pad pitch of the two first connected pads in the corner is less than 120 µm. The two first pads must be connected to the same lead.

Case B:

The pad pitch of the two firsts pads in the corner is more than 120 µm. The two first pads can be connected to two different leads.

3. Other minimum dimensions



A: Street width

B: Bond pad metal to scribe line

C: Bond pad metal to active adjacent metal

D: Bond pad metal to grid metal

A (µm)	B (µm)	C (µm)	D (µm)
80	50	10	25

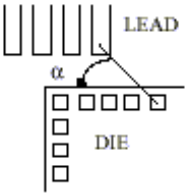
4. Wire rules

4.1. Wire angle:

The wire angle α between wire axis and die edge is package dependent:

All packages: 30-90°

except Super BGA: 45-90°



4.2. Wire length:

The wire length is package dependent. The length is measured in a horizontal plan from bond pad within 200 µm of package finger.

a) Plastic package:

The maximum wire length is the following:

PQFP, LQFP, TQFP, BGA and PLCC: 4.5 mm

SOIC and PDIP: 3.3 mm

b) Ceramic package:

Volume production:

Side-braze, chip carrier, cerdip, cerquad, quad flat pack, PGA: 4.0 mm

For a double deck package: internal row: 4.0 mm

external row: 5.0 mm

Prototype production:

Side-braze, chip carrier, cerdip, cerquad, quad flat pack, PGA: 5.0 mm

For a double deck package: internal row: 5.0 mm

external row: 6.0 mm

4.3. Distance between wire:

The distance between wire, from axis to axis, is pad pitch dependent.

Pad pitch (µm)	Minimum distance (µm)
>100	100
90	60
80-75	50

For a double deck package:

60 µm minimum between wires from the same deck

No crossing between wires from different deck

4.4. Wire over lap:

Wire cannot cross over more than 500 µm of the die

4.5. Down bond:

When a down bond is required, a minimum of 1 mm must be left between the die edge and the cavity edge.

Some package cannot accept a down bond. This option should be checked with the assembly department.

5. Bonding diagram

- It must be in conformance with specification AG4-AO05.
- Bonding diagram must come from Fast V400 in order to check all assembly rules.
- Location of ID block must be shown. **ID block must contain product number.**

6. Maximum current per wire

A maximum of 700 milliamps per wire is allowed.

Appendix C

BTI pad placement file

```
**********************************************************************
**** **** *** *  S I L I C O N   W O R K   O R D E R S                 *
**    *** *** ***************************************************
***** **** **** *  D E V I C E   P I N - O U T   S H E E T            *
**********************************************************************
*   DATE          * PACKAGE TYPE        * PRODUCT No          *
*   25/ 3/1997    *    TQ064VS          *   btitop                   *
*                 *                     *                            *
*-------------------------------------------------------------------------
      *
*                                                    PAD CENTRE       *
*BNDPAD FT  PT    PIN          ES2 DATA  PIN CUST   COORDINATES       *
*PIN   PIN  PIN PIN FUNC       SHEET     NAME          (um)           *
*-------------------------------------------------------------------------
      *
* 1              GNDC        PC45FREUR  Vssi        2031, -1703      *
* 2              GNDC        PC45FREUR  VssAC       2031, -1601      *
* 3              VDDC        PVDA       VddAC       2031, -1280      *
* 4              GNDX        PV0A       VssAC       2031, -1181      *
* 5              I           PC3D21U    prgb        2031, -884       *
* 6              GNDC        PV0D       VssDC       2031, -694       *
* 7              VDDC        PVDD       VddDC       2031, -397       *
* 8              I           PC3D21D    phi         2031, -187       *
* 9              I           PC3D21D    ck          2031, 0          *
* 10             GNDC        PV0D       VssDC       2031, 187        *
* 11             VDDC        PVDD       VddDC       2031, 595        *
* 12             I           PC3D21U    snprstb     2031, 695        *
* 13             VDDC        PVDA       VddAC       2031, 884        *
* 14             GNDC        PV0I       Vssi        2031, 1181       *
* 15             VDDC        PVDI       Vddi        2031, 1281       *
* 16             VDDC        PC45FREUL  VddDC       2031, 1703       *
* 17             NC                                                  *
* 18             VDDC        PC45FREUL  Vddi        1771, 1863       *
* 19             VDDC        PC45FREUL  VddAC       1678, 1863       *
* 20             I/O         PC3B03D    w1          1281, 1863       *
* 21             I/O         PC3B03D    w2          1113, 1863       *
```

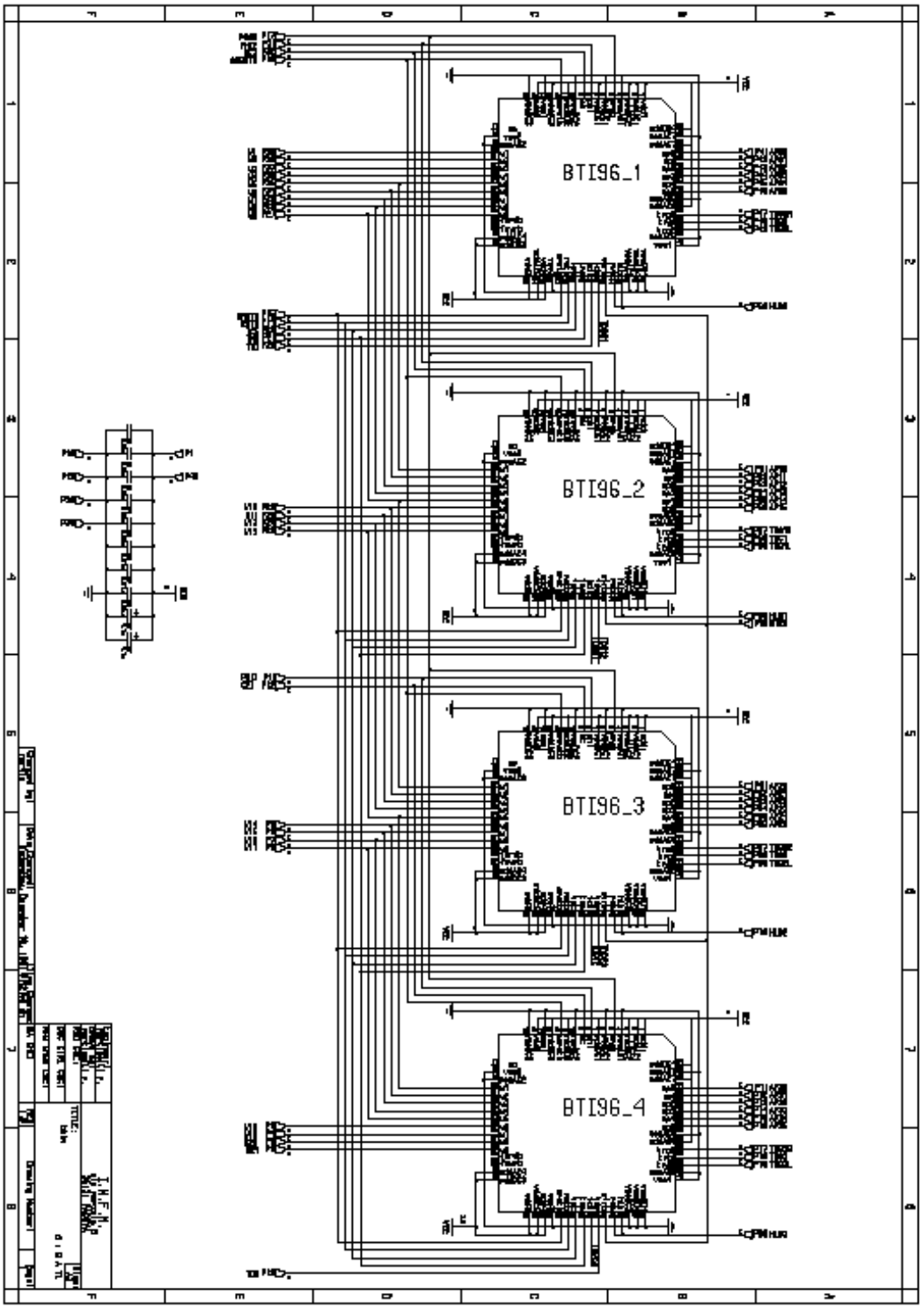
* 22	I/O	PC3B03D	w3	833, 1863	*
* 23	I/O	PC3B03D	w4	555, 1863	*
* 24	I/O	PC3B03D	w5	277, 1863	*
* 25	I/O	PC3B03D	w6	-1, 1863	*
* 26	I	PC3D01D	w7	-277, 1863	*
* 27	I	PC3D01D	w8	-555, 1863	*
* 28	I	PC3D01D	w9	-834, 1863	*
* 29	O	PC3O03	ferdb	-1111, 1863	*
* 30	O	PC3O03	fewrb	-1288, 1863	*
* 31	GNDC	PC45FRELL	VssAC	-1678, 1863	*
* 32	GNDC	PC45FRELL	VssDC	-1771, 1863	*
* 33	GNDC	PC45FRELL	Vssi	-2031, 1703	*
* 34	GNDC	PC45FRELL	VssAC	-2031, 1601	*
* 35	VDDC	PVDI	Vddi	-2031, 1236	*
* 36	GNDC	PV0I	Vssi	-2031, 1101	*
* 37	I	PC3D21U	sresetb	-2031, 855	*
* 38	I	PC3D21U	resetb	-2031, 602	*
* 39	I	PC3D21D	tck	-2031, 357	*
* 40	I	PC3D21U	tms	-2031, 121	*
* 41	I	PC3D21U	tdi	-2031, -121	*
* 42	TRI	PC3T01U	tdo	-2031, -355	*
* 43	I	PC3D21U	strb	-2031, -602	*
* 44	I	PC3D21U	rwb	-2031, -855	*
* 45	TRI	PC3T04D	hlb	-2031, -1100	*
* 46	GNDX	PV0A	VssAC	-2031, -1233	*
* 47	VDDC	PC45FRELR	VddAC	-2031, -1601	*
* 48	VDDC	PC45FRELR	VddDC	-2031, -1703	*
* 49	VDDC	PC45FRELR	Vddi	-1771, -1863	*
* 50	VDDC	PC45FRELR	VddAC	-1678, -1863	*
* 51	TRI	PC3T04D	trg2	-1318, -1863	*
* 52	TRI	PC3T04D	trg1	-1181, -1863	*
* 53	TRI	PC3T04D	trg0	-854, -1863	*
* 54	VDDC	PVDA	VddAC	-605, -1863	*
* 55	GNDX	PV0A	VssAC	-465, -1863	*
* 56	I/O	PC3B04D	ap5	-228, -1863	*
* 57	I/O	PC3B04D	ap4	-1, -1863	*
* 58	I/O	PC3B04D	ap3	228, -1863	*
* 59	I/O	PC3B04D	ap2	467, -1863	*
* 60	I/O	PC3B04D	ap1	605, -1863	*
* 61	I/O	PC3B04D	ap0	853, -1863	*
* 62	VDDC	PVDA	VddAC	1181, -1863	*
* 63	GNDX	PV0A	VssAC	1330, -1863	*
* 64	GNDC	PC45FREUR	VssDC	1771, -1863	*
* NC	NC	I308	VddAC	2042, 1601	*

* NC	NC	I249	Vssi	2042, 397	*
* NC	NC	I250	Vssi	2042, -597	*
* NC	NC	I309	VssAC	1679, -1964	*

****

Appendix D

BTIM schematic



Appendix E

BTIM socket drawing