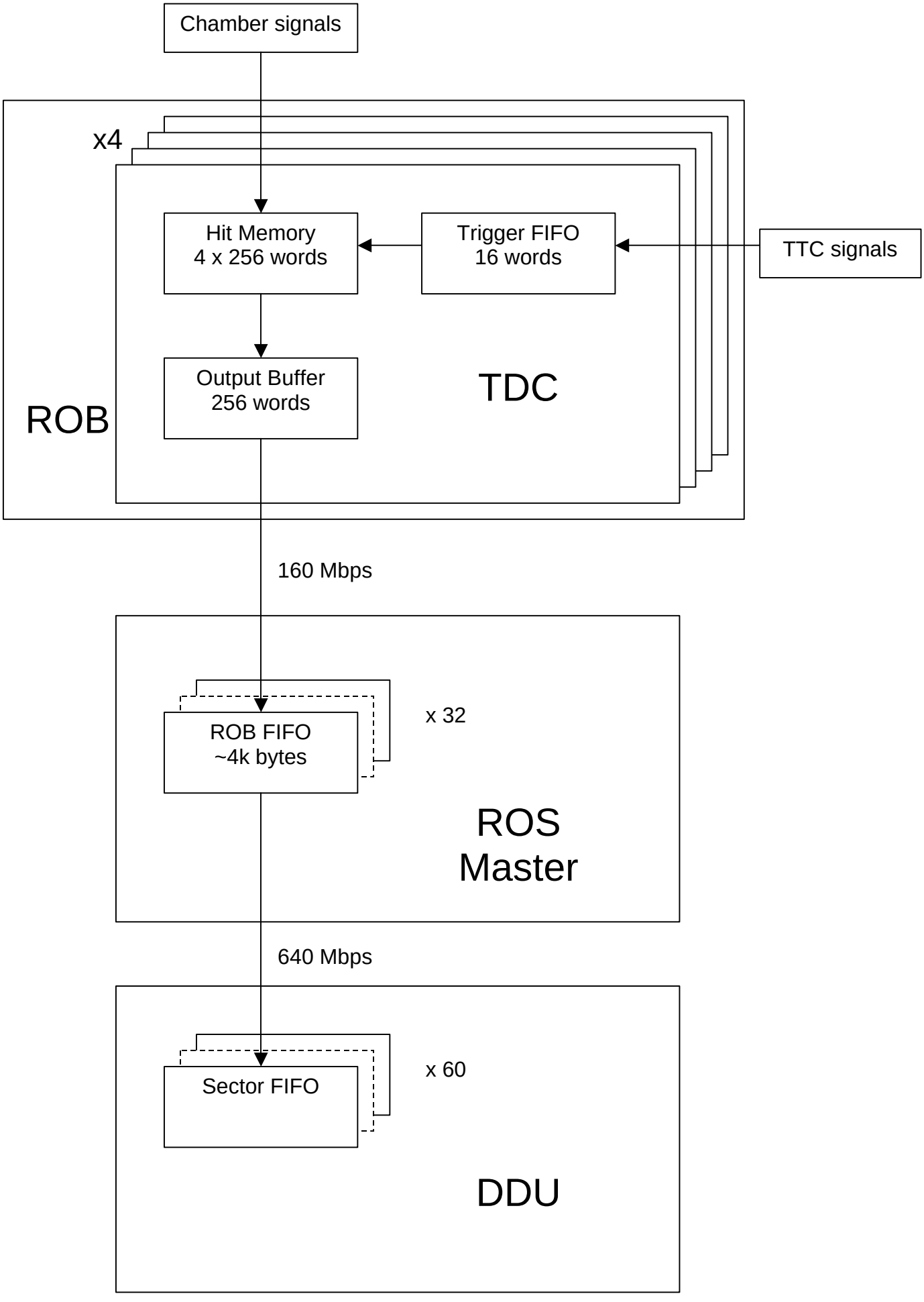
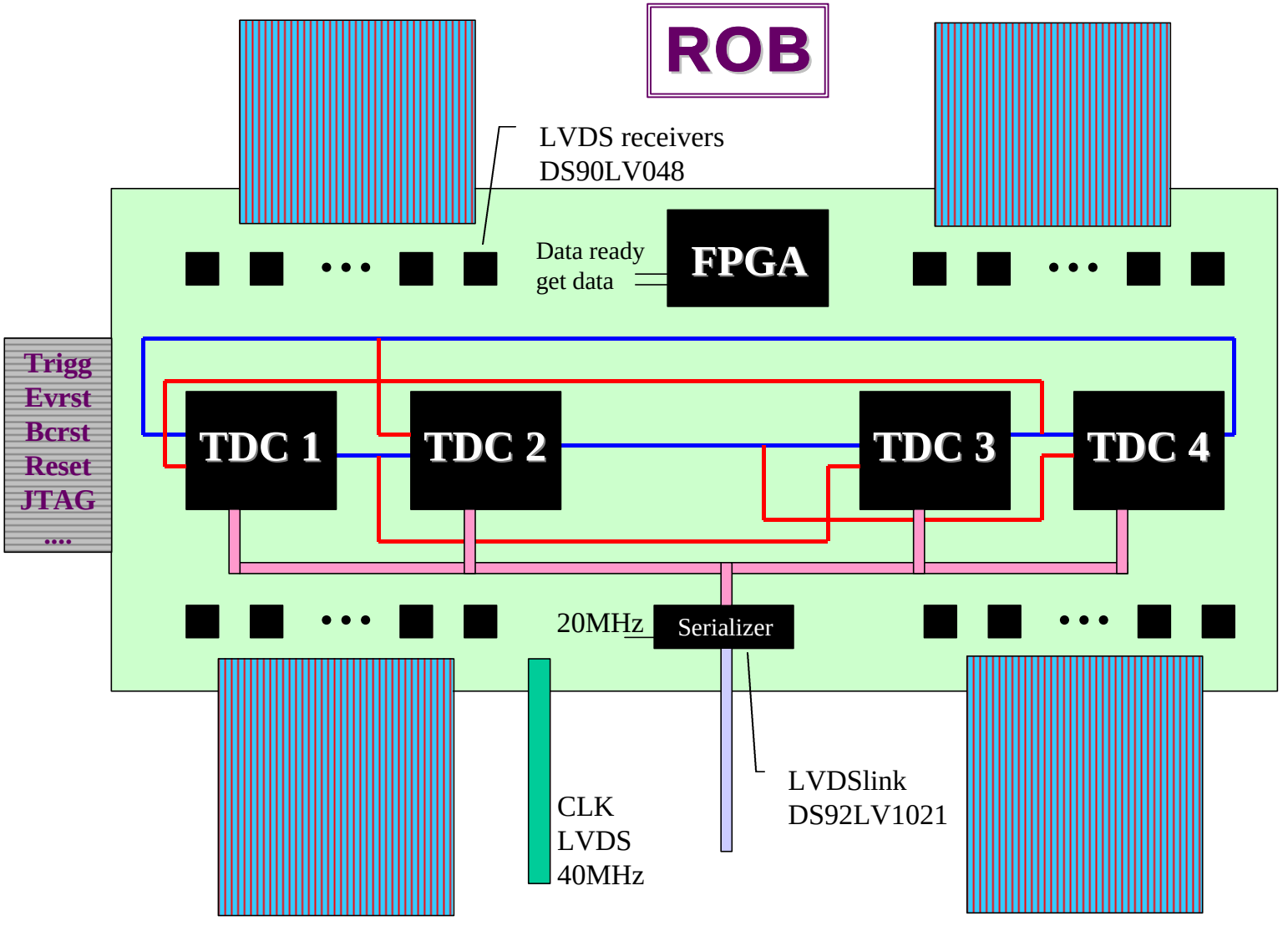
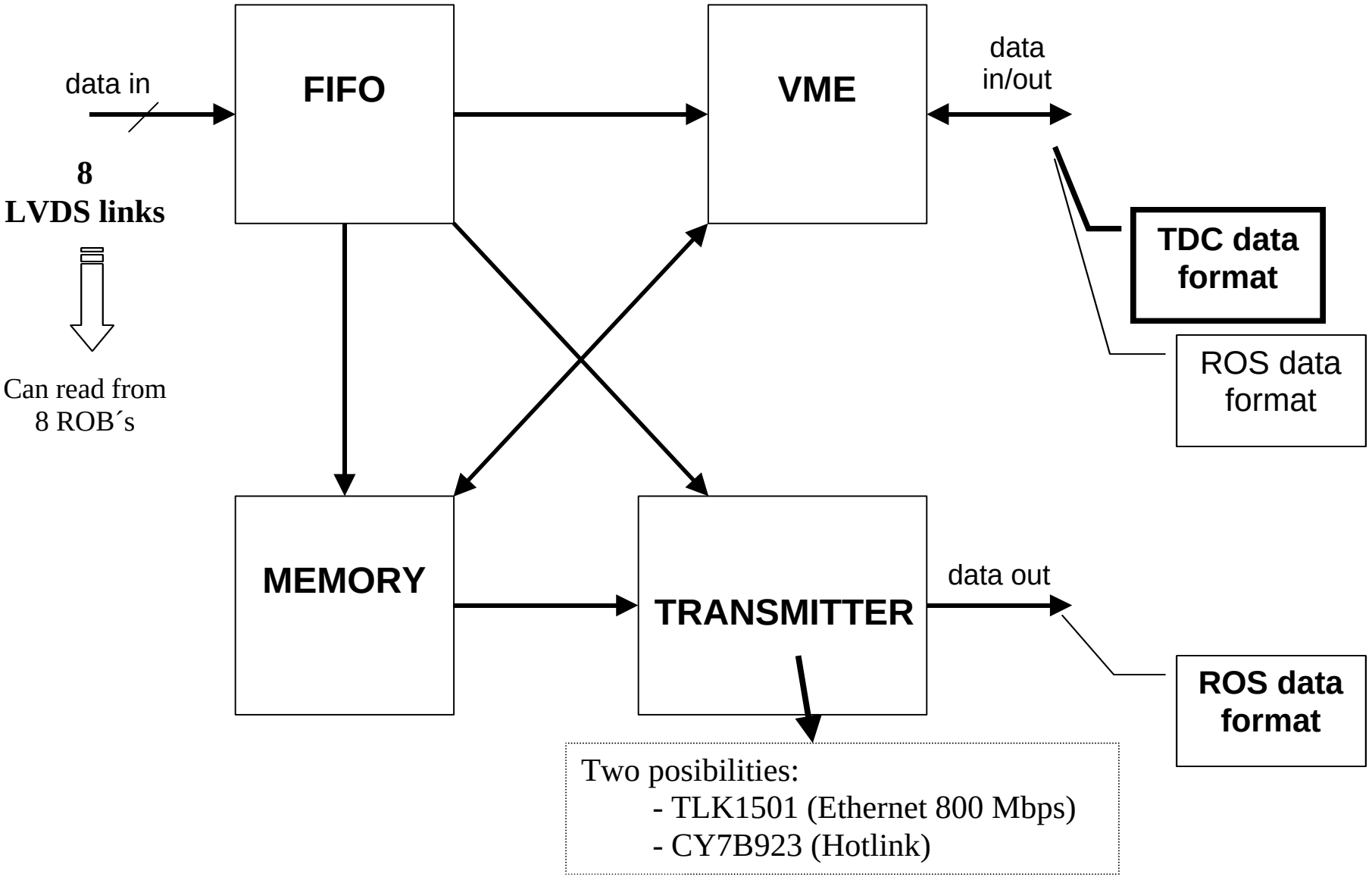
READOUT SYSTEM AND MINICRATE OPERATION

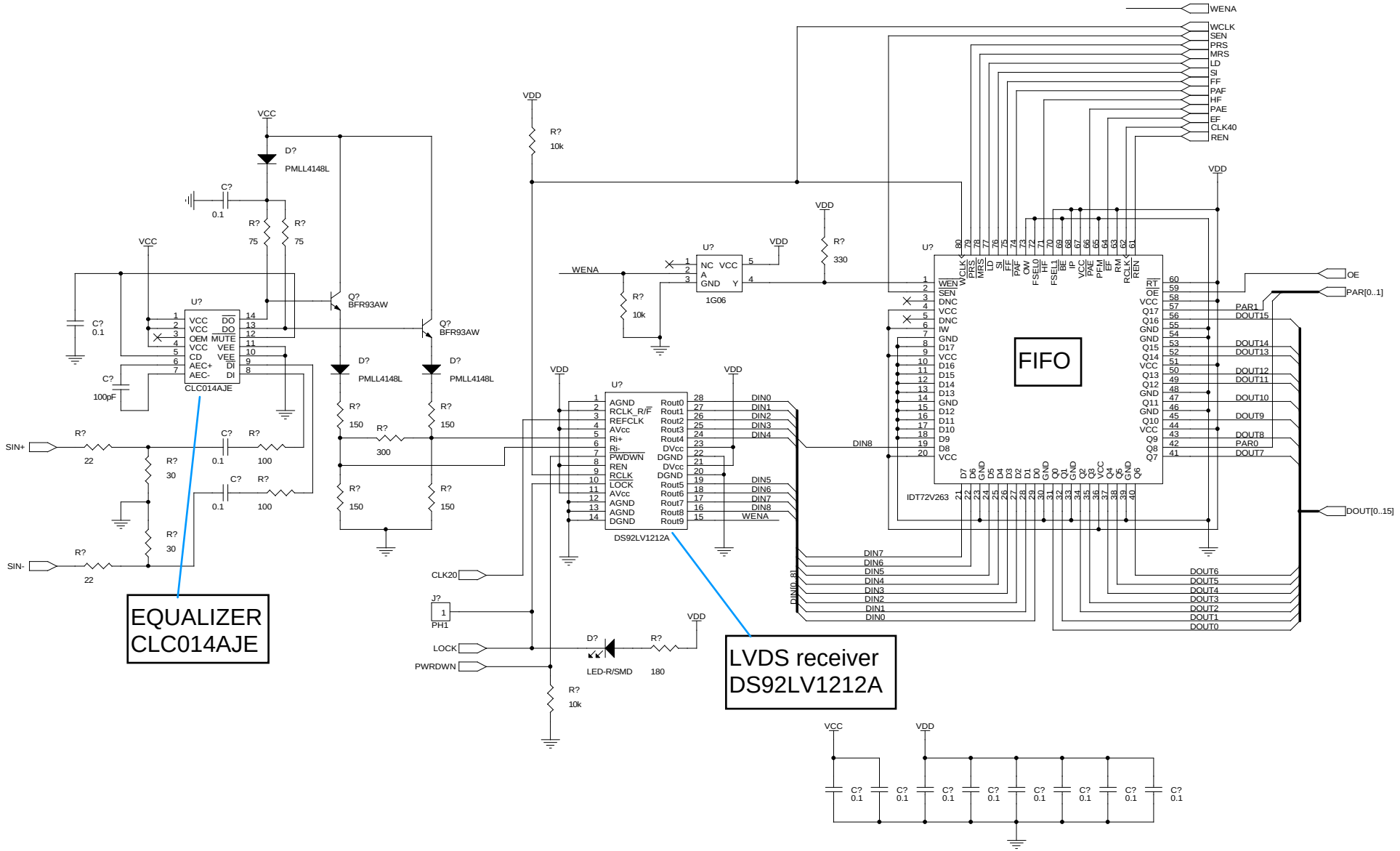
- Description of the READOUT SYSTEM:
  - * ROB
  - * ROS
- Data formats.
- Control-x board: Functionality.
- Patgen: Description.
- Minicrate readout operation:
  - * List of components.
  - * Software for Slow Control and Readout.


Chamber signals
x4
Hit Memory
4 x 256 words
Trigger FIFO
16 words
TTC signals
Output Buffer
256 words
TDC
ROB
160 Mbps
ROB FIFO
~4k bytes
x 32
ROS
Master
640 Mbps
Sector FIFO
x 60
DDU


ROB
LVDS receivers
DS90LV048
Data ready
get data
FPGA
Trigg
Evrst
Bcrst
Reset
JTAG
....
TDC 1
TDC 2
TDC 3
TDC 4
20MHz
Serializer
CLK
LVDS
40MHz
LVDSlink
DS92LV1021

ROS-8 BLOCK DIAGRAM





Las señales SIN+ y SIN- son diferenciales (200 Mbps) y deben ir juntas y aisladas del resto de las demás señales.

Hay que minimizar el recorrido de las señales que van de los pines 13 y 14 del circuito CLC014 a los pines 5 y 6 del circuito DS92LV1212A.
Estas señales son diferenciales.

Title: ROS-8 / MODULO		
Size: A3	Document Number	Rev: A
Date: Wednesday, November 21, 2001	Sheet 4 of 9	

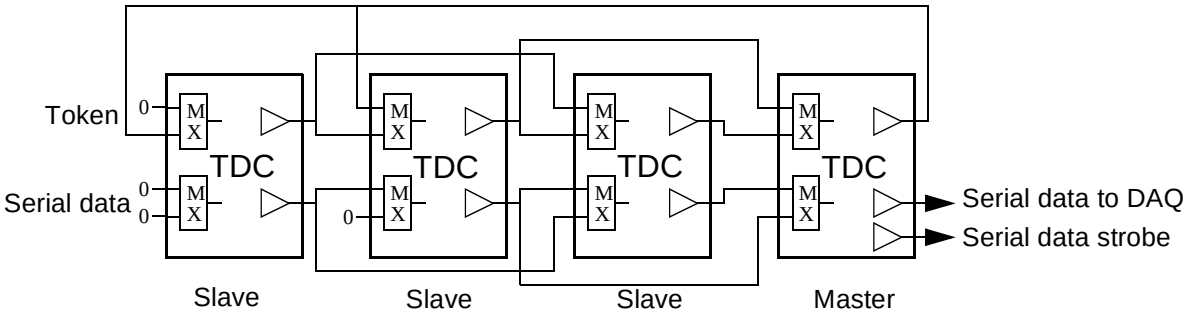


Fig. 16 Serial connection of TDC's with option of bypassing failing slave TDC

13.6. JTAG read-out

For debugging purposes a read-out interface is also available via JTAG. In this read-out mode the token passing between TDCs are disabled and individual words can be read from the JTAG read-out path. A status bit in the data read indicates if a data word was in fact ready for read-out. Each word read is removed from the read-out fifo to be capable of reading subsequent data.

13.7. Packet format

Data read out of the TDC is contained in 32 bit data packets. The first four bits of a packet are used to define the type of data packet. The following 4 bits are used to identify the ID of the TDC chip (programmable) generating the data. Only 8 out of the possible 16 packet types are defined for TDC data (bit 31 always set to zero by TDC). The remaining 8 packet types are available for data packets added by higher levels of the DAQ system.

Group header: Event header from master TDC

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	TDC				Event ID												Bunch ID											

TDC: Programmed ID of master TDC.
Event ID: Event ID from event counter.
Bunch ID: Bunch ID of trigger (trigger time tag).

Group trailer: Event trailer from master TDC

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	TDC				Event ID												Word count											

TDC: Programmed ID of master TDC.
Event ID: Event ID from event counter.
Word count: Total number of words in event (incl. headers and trailers).

TDC header: Event header from TDC (master and slaves)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	TDC				Event ID												Bunch ID											

TDC: Programmed ID of TDC.
Event ID: Event ID from event counter.

Bunch ID: Bunch ID of trigger (trigger time tag).

TDC trailer: Event trailer from TDC (master and slaves)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	TDC				Event ID												Word count											

TDC: Programmed ID of TDC.
Event ID: Event ID from event counter.
Word count: Number of words from TDC (incl. headers and trailers).

Leading measurement:

Single edge

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	TDC				Channel					Leading time																		

TDC: Programmed ID of TDC.
Channel TDC channel number.
Leading: Leading edge measurement in programmed resolution

Combined measurement of leading and trailing edge

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	TDC				Channel					Width							Leading time											

TDC: Programmed ID of TDC.
Channel: TDC channel number.
Width: Width of pulse in programmed time resolution.
Leading: Leading edge in programmed time resolution

Trailing measurement:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	TDC				Channel					Trailing time																		

TDC: Programmed ID of TDC.
Channel TDC channel number.
Trailing: Trailing edge measurement in programmed resolution

Errors: Error flags sent if an error condition has been detected

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	0	TDC													Error flags														

TDC: Programmed ID of TDC.
Error flags:

[0]: Hit lost in group 0 from read-out fifo overflow.
[1]: Hit lost in group 0 from L1 buffer overflow
[2]: Hit error have been detected in group 0.
[3]: Hit lost in group 1 from read-out fifo overflow.
[4]: Hit lost in group 1 from L1 buffer overflow
[5]: Hit error have been detected in group 1.
[6]: Hit data lost in group 2 from read-out fifo overflow.
[7]: Hit lost in group 2 from L1 buffer overflow
[8]: Hit error have been detected in group 2.
[9]: Hit lost in group 3 from read-out fifo overflow.
[10]: Hit lost in group 3 from L1 buffer overflow
[11]: Hit error have been detected in group 3.
[12]: Hits rejected because of programmed event size limit
[13]: Event lost (trigger fifo overflow).
[14]: Internal fatal chip error has been detected.

Debugging data: Additional information for system debugging

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	1	TDC				Sub type																							

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	1	TDC				0	0	0	0									Bunch ID											

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	1	TDC				0	0	0	1											GR		L1 occupancy							

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	1	TDC				0	0	1	0								Trigger fifo				F	Read-out fifo							

TDC: Programmed ID of TDC.
Sub type: Debugging data sub type:
0000: separator
0001: L1 Buffer occupancy (one for each of the four groups)
0010: Trigger and read-out fifo occupancy
Bunch ID: Trigger time tag counter when separator was generated.
L1 occupancy: L1 buffer occupancy.
GR: Channel Group.
Trigger fifo: Trigger fifo occupancy

Generated at TDC, modified by ROS Master

Group header: event header from master TDC (one per ROB)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDC	0	0	0	0	TDC ID				Event ID												Bunch ID											
ROS	0	0	0	ROB ID (0-30)					Event ID												Bunch ID											
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Group trailer: event trailer from master TDC (one per ROB)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDC	0	0	0	1	TDC ID				Event ID												Word count											
ROS	0	0	1	ROB ID (0-30)					Event ID												Word count											
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

TDC header: event header from TDC (master and slaves)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDC	0	0	1	0	TDC ID				Event ID												Bunch ID											
ROS	0	1	0	0	0	0	TDC ID		Event ID												Bunch ID											
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

TDC trailer: event trailer from TDC (master and slaves)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDC	0	0	1	1	TDC ID				Event ID												Word count											
ROS	0	1	1	0	0	0	TDC ID		Event ID												Word count											
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Leading measurement: single edge (normal time measurement)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDC	0	1	0	0	TDC ID				Channel					Leading time																		
ROS	1	0	0	0	0	0	TDC ID		Channel					Leading time																		
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Leading measurement: combined measurement of leading and trailing edge

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDC	0	1	0	0	TDC ID				Channel					Width							Leading time											
ROS	1	0	0	0	0	0	TDC ID		Channel					Width							Leading time											
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Trailing measurement

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDC	0	1	0	1	TDC ID				Channel					Trailing time																		
ROS	1	0	1	0	0	0	TDC ID		Channel					Trailing time																		
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Errors: error flags sent when error condition is detected

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDC	0	1	1	0	TDC ID													Error flag														
ROS	1	1	0	0	0	0	TDC ID											Error flag														
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Debugging data: separator

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDC	0	1	1	1	TDC ID				0	0	0	0									Bunch ID											
ROS	1	1	1	0	0	0	TDC ID		0	0	0	0									Bunch ID											
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Debugging data: L1 buffer occupancy

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDC	0	1	1	1	TDC ID				0	0	0	1											GR	L1 occupancy							
ROS	1	1	1	0	0	0	TDC ID		0	0	0	1											GR	L1 occupancy							
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Debugging data: trigger and readout fifo occupancy

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDC	0	1	1	1	TDC ID															Trigger fifo				F	Read-out fifo							
ROS	1	1	1	0	0	0	TDC ID													Trigger fifo				F	Read-out fifo							
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Generated at ROS Master

Event header: event header from ROS Master

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ROS	0	0	0	1	1	1	1	1	ROS event ID								TTC L1A ID															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Event trailer: event trailer from ROS Master

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ROS	0	0	1	1	1	1	1	1	ROS event ID								Word count															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Errors: error flags sent when error condition is detected

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ROS	1	1	0	1	1	1	1	1	Error type			Link/ROB ID																				
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Error types:

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Link unlocked			Link ID																				
1	Link time out			Link ID																				
2	Group Event misalignement			Link ID					expected Event ID								found Event ID							
3	Parity error			Link ID																				
4	Fifo almost full			Link ID																				
5	Fifo full			Link ID																				
	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Status: status from ROS Master (once every n events)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ROS	1	1	1	1	1	1	1	1	0	0	0	Link 6			Link 5			Link 4			Link 3			Link 2			Link 1			Link 0		
ROS	1	1	1	1	1	1	1	1	0	0	1	Link 13			Link 12			Link 11			Link 10			Link 9			Link 8			Link 7		
ROS	1	1	1	1	1	1	1	1	0	1	0	Link 20			Link 19			Link 18			Link 17			Link 16			Link 15			Link 14		
ROS	1	1	1	1	1	1	1	1	0	1	1	Link 27			Link 26			Link 25			Link 24			Link 23			Link 22			Link 21		
ROS	1	1	1	1	1	1	1	1	1	0	0	Spare			Spare			Spare			Spare			Link 30			Link 29			Link 28		
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Link info:

	2	1	0
Link n	Unlocked	Time Out	Masked

ROS Registers

All accesses A24

Memory Access (Word)

Address 0 - 262143

0-15	Memory Data	R/W

Register Access (Long Word)

Register 0

GRP00-00 (00 00 00)
General Control & Status

0-1	00 → Interrupt Disable 01 → Enable SPAE 10 → Enable SPAF 11 → Enable End of Memory	R/W
2	Serializer Power Up	R/W
3	Fifo to Serializer	R/W
4	SPAE	R
5	SPAF	R
6	Memory Done Memory to Serializer	R W
7	Select Veto 0 → SPAE / 1 → SPAF	R/W
8	Master Fifo Reset	W
9	Partial Fifo Reset	W
10	Load FIFO's Programmed Values	W
11	Board Reset	W

Register 1

GRP00-01 (00 00 01)
Receiver Control & Status

0-7	Receiver Power Up 1-8	R/W
8-15	Receiver Lock 1-8	R

Register 2

GRP00-10 (00 00 10)
Programmed PAE Value

0-12	PAE	R/W

Register 3

GRP00-11 (00 00 11)
Programmed PAF Value

0-12	PAF	R/W

Register 5

GRP01-01 (00 01 01)
FF Status

0-7	FF Fifo 1-8	R
8-15	FF Latched Fifo 1-8	R

Register 6

GRP01-10 (00 01 10)
PAE & PAF Status

0-7	PAE Fifo 1-8	R
8-15	PAF Fifo 1-8	R

Register 7

GRP01-11 (00 01 11)
EF & HF Status

0-7	EF Fifo 1-8	R
8-15	HF Fifo 1-8	R

Register 8

GRP10-00 (00 10 00)
Interrupt

0-7	Interrupt Vector	R/W
8-10	Interrup Level 1-7	R/W

Register 9

GRP10-01 (00 10 01)
Memory Address Pointer

0-17	Memory Address Pointer	R/W

Register 12

GRP11-00 (00 11 00)
Transmission Status 1 & Control

0-7	Channel Time Out 1-8	R
8-15	Mask Channel 1-8	R/W

Register 13

GRP11-01 (00 11 01)
Transmission Status 2

0-15	Last Event Number	R

Register 16-23

GRP2 (010 XXX)
Data Fifo 1-8

0-15	Fifo 1-8 Data 0-15	R
16-17	Fifo 1-8 Parity 0-1	R
18	Fifo 1-8 Parity Error	R
19	Fifo 1-8 EF	R
20	Fifo 1-8 FF	R
21	Fifo 1-8 PAE	R
22	Fifo 1-8 PAF	R

Register 24-31

GRP3 (011 XXX)
Read Sequentially PAE & PAF FIFO Values

0-12	PAE / PAF Values FIFO 1-8	R

Register 32-39

GRP4 (100 XXX)
FIFO byte count

0-16	Byte count FIFO 1-8	R/W

PATGEN

- 2 LVDS inputs for test pulses (p0 and p1)
- 128 LVDS output channels
- Each channel can be independently enabled/masked for p0, p1 or both.
- One patgen can deliver data for every channel of a ROB-128.

CONTROL-X

- 40 MHz clock

  Input: internal clock, NIM, TTL
  Output: 8 LVDS, 1 LVPECL

- 2 NIM inputs for interruption (beginning/end spill)

- Output trigger:

  * ***non-synchronized*** (T0): (no veto)
    Input: NIM, TTL or VME.

  * ***synchronized*** (programmable delay, veto)
    Input: NIM, TTL, or VME
    Output: NIM, LVDS, LVDS (ROBUS), LVPECL

- 2 LVDS output test pulses: (p0 and p1)
  programmable 0.5 ns step delay
  Input: TTL, VME.

- Trigger Veto:
  Input: LVDS

- ROB Reset:
  Input: TTL, VME
  Output: LVDS (ROBUS)

- Event Reset, Bunch Reset :
  Input: TTL, VME
  Output: LVEPCL, LVDS(ROBUS)

LIST OF COMPONENTS FOR A MINICRATE (READOUT SCHEDULE)

ROB-128

- 30 final PCB produced
- 10 boards assembled with HPTDC v1.2
- These boards will be fully tested in June-October
- Exercise final test programme for production
- Enough boards with HPTDC v1.1 to equip 2 full minicrates.

ROS-8

- Each board is able to read one full minicrate.
- Problems with company designing PCB: expected in May but still to be delivered. New date mid July.
- Assembled and tested boards will be available in September.

MINICRATE MECHANICS

- Two MB1 ready.
- Two MB2 are in process.

We can also provide:

- Patgen:
  - * They distribute pulses simultaneously to every selected ROB channel.
  - * Necessary one per ROB.
  - * Now 2 units available. 10 more can be produced in short time.
- Control-X:
  - * Synchronizes trigger, programmable trigger delay, 50 ns pulses generation, spill interruptions management, trigger veto, up to 8 LVDS 40

MHz clock signals, bunch reset, event reset, etc.

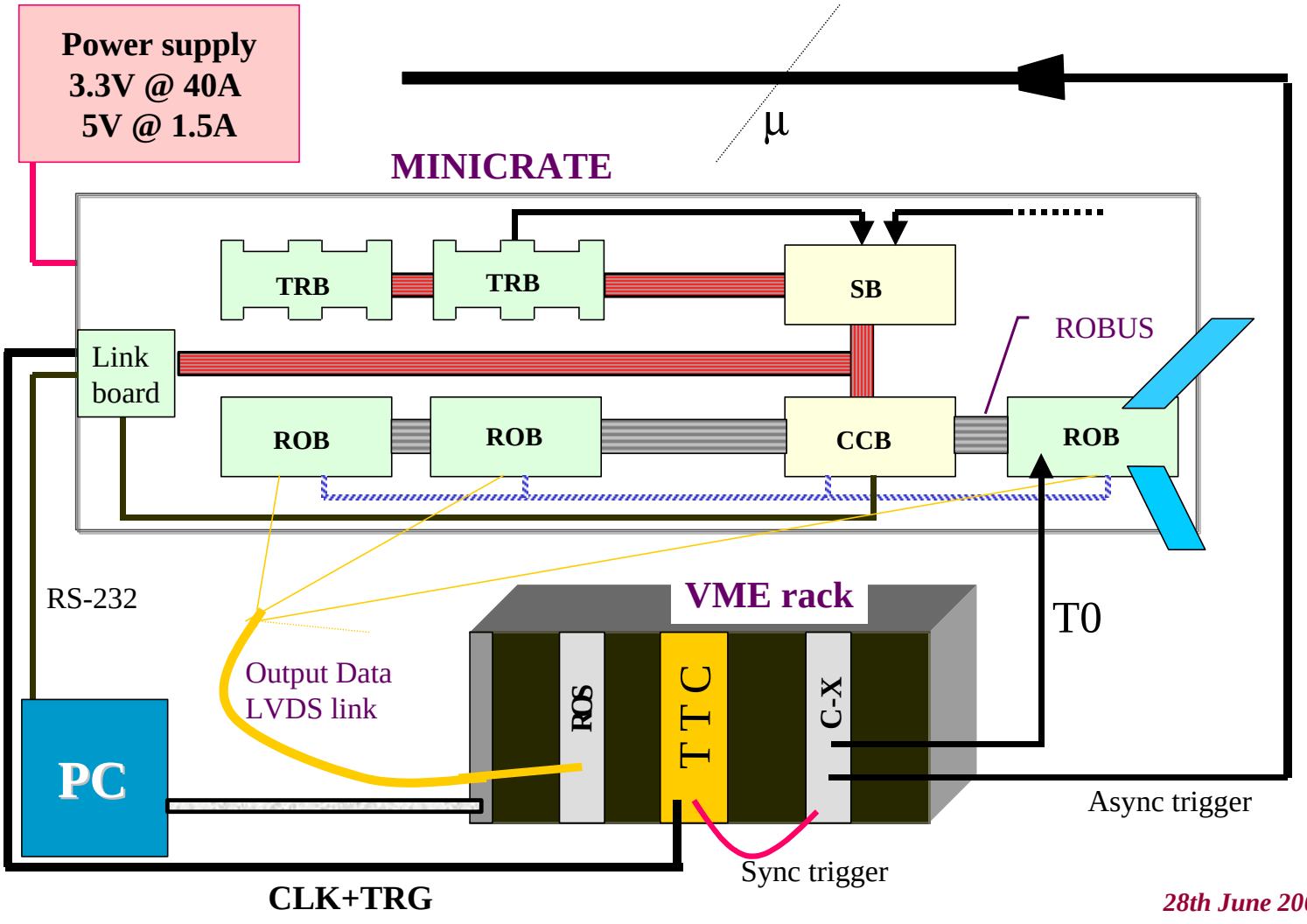
* Two boards available. If necessary 2 more could be assembled in short time.

Other necessary items:

- Link board
- PC
- VME rack
- VME-PC interface or similar.
- Trigger system for cosmic rays: plastics, ...
- TTC system

Ciemat

RO MINICRATE OPERATION



28th June 2002

SLOW CONTROL SOFTWARE (J.C. Oller)

MC68HC16 software modifications:

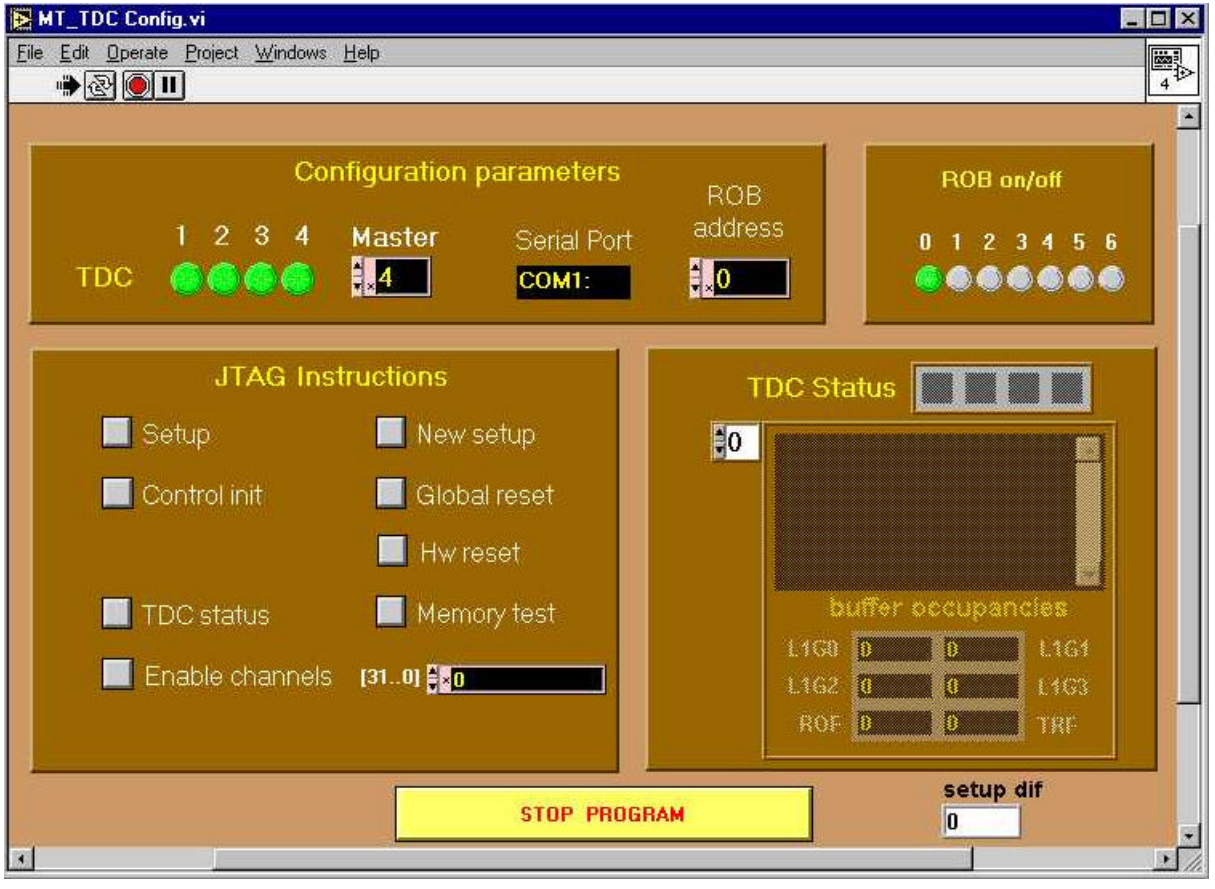
- We have included three JTAG instructions for TDC control and configuration:
  - * JTAG_SETUP
  - * JTAG_CONTROL
  - * JTAG_STATUS
  - * Also a command for ROB power up.
- Other instructions shall be implemented: TDC bypass...

LabView sotfware for user interface:

- Communicates with the MC68HC16 via RS-232.
- Sends the desired command and the necessary parameters.

READ-OUT SOFTWARE

- There is a programm for one ROB data acquisition, with Control-X and Patgen.
- Makes use of NI-VXI libraries for LabView.
- It has to be adapted for ROS operation, ...

SLOW CONTROL:

ROB turn-on, TDC set-up and status monitorization