The Readout System

- HPTDC
- ROB
- ROS Master
- DDU
- Data Links
- Error Monitoring

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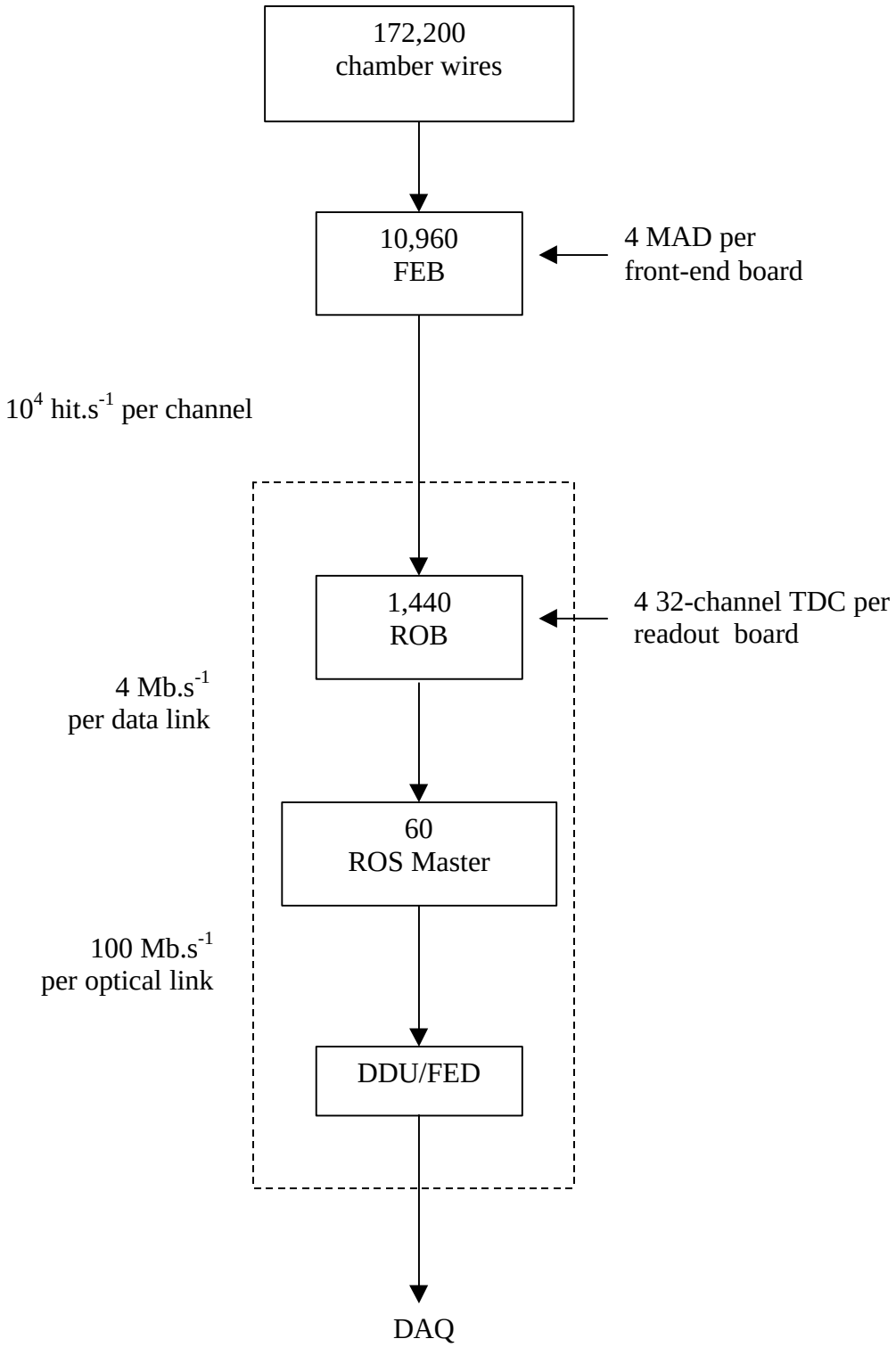
DT Readout system overview



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HPTDC

http://micdigital.web.cern.ch/micdigital/hptdc.htm

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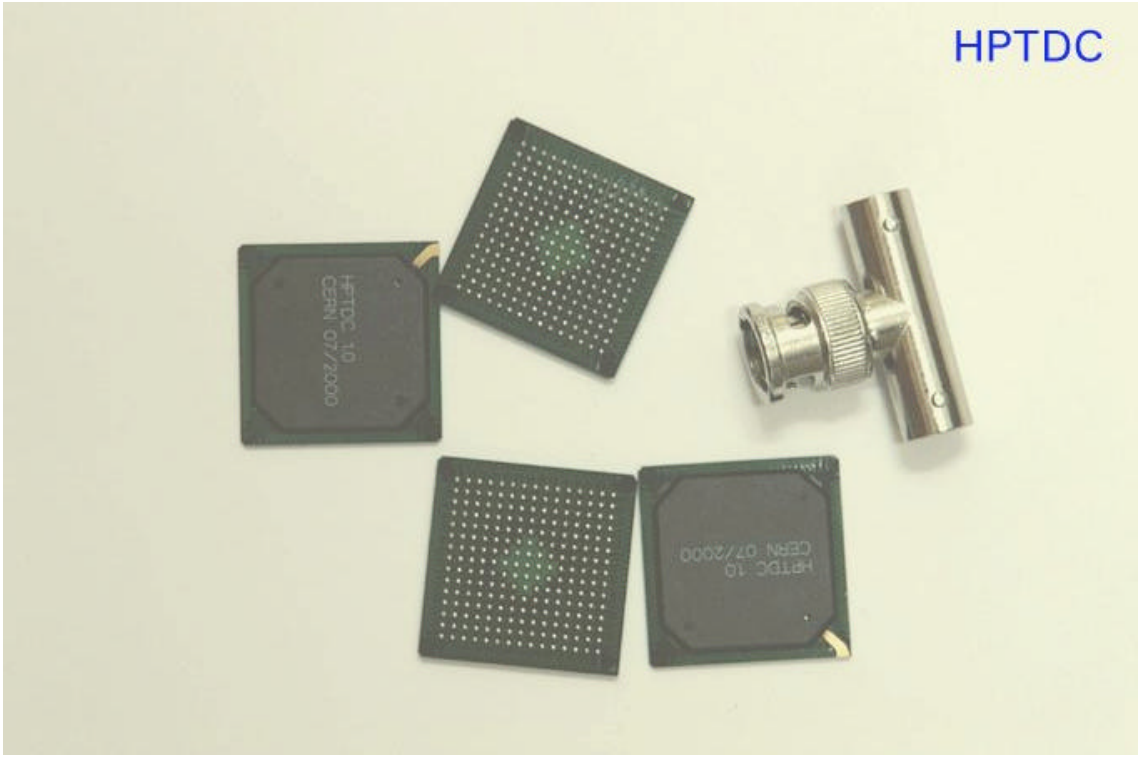

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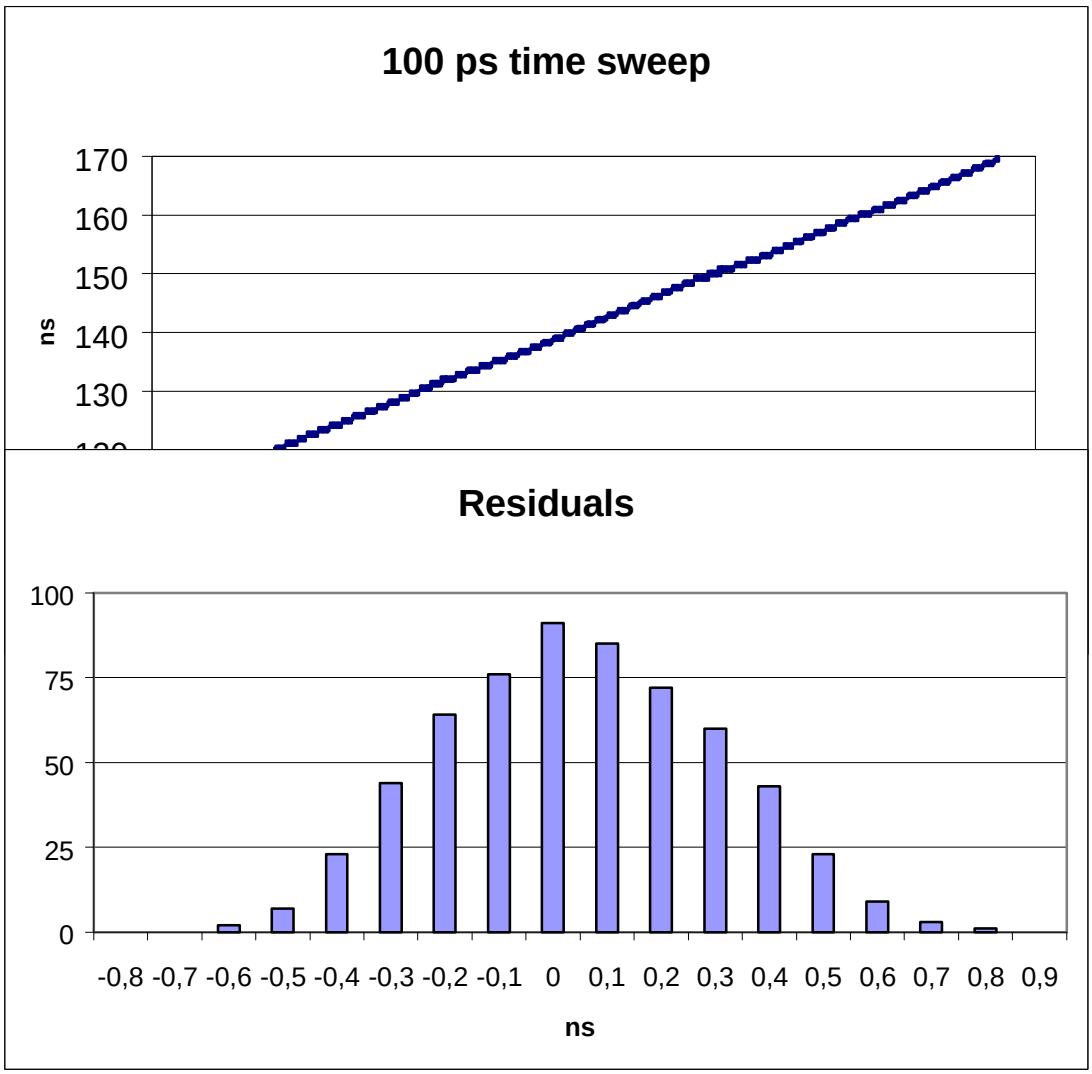
100 ps time sweep
170
160
150
140
130
ns
Residuals
100
75
50
25
0
-0,8 -0,7 -0,6 -0,5 -0,4 -0,3 -0,2 -0,1 0 0,1 0,2 0,3 0,4 0,5 0,6 0,7 0,8 0,9
ns

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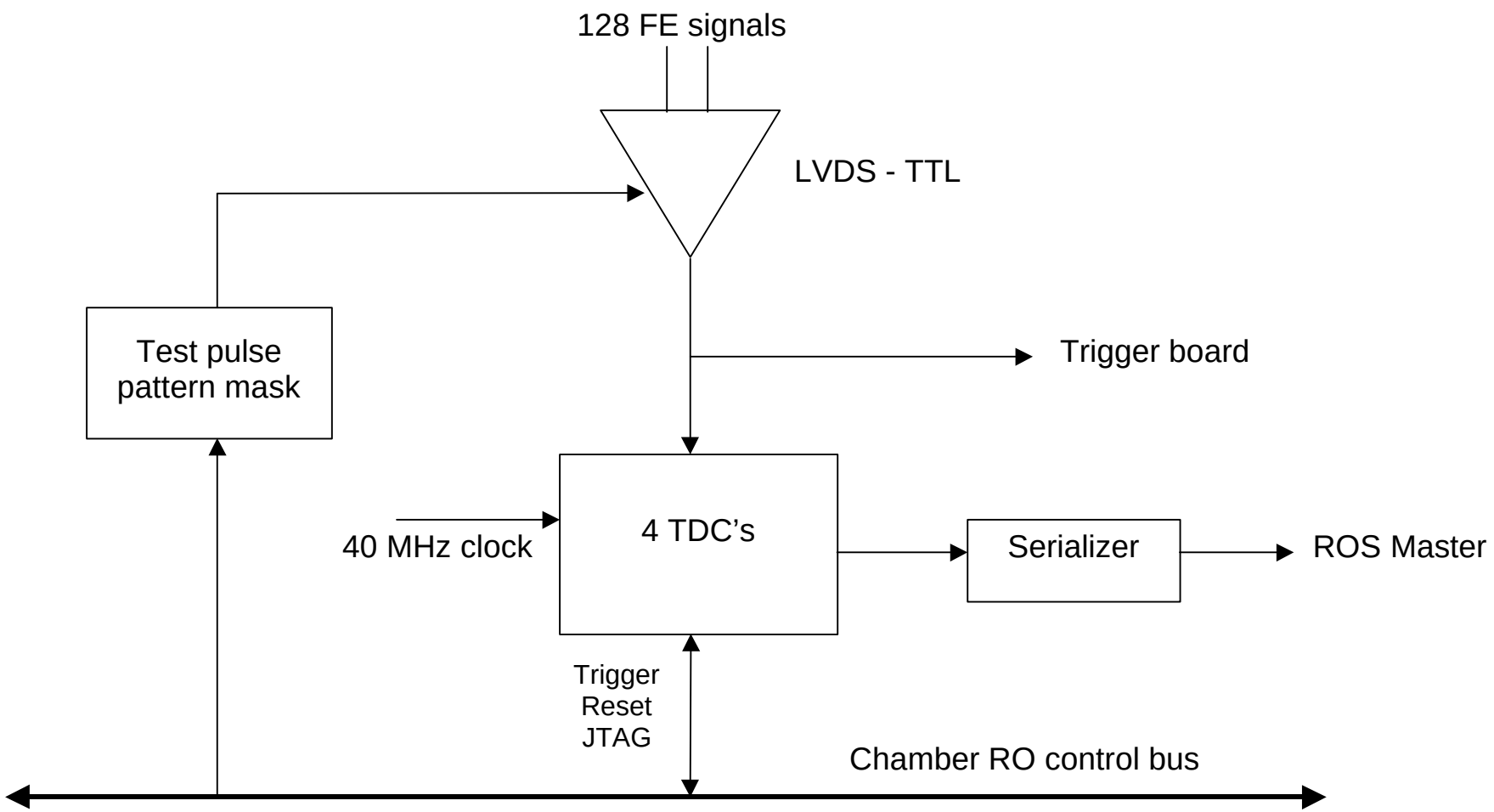
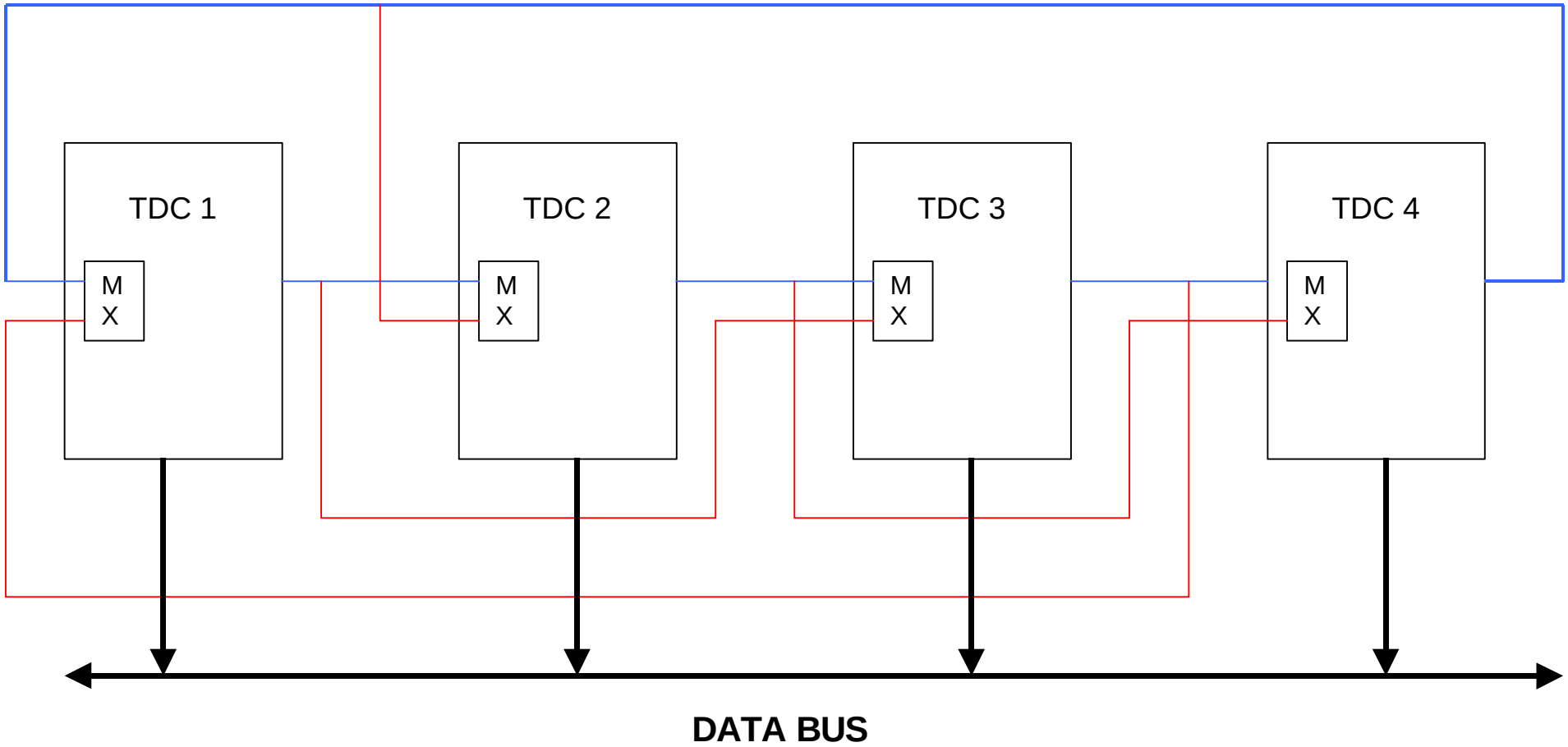
ROB Block Diagram



4 HPTDC token ring with bypass



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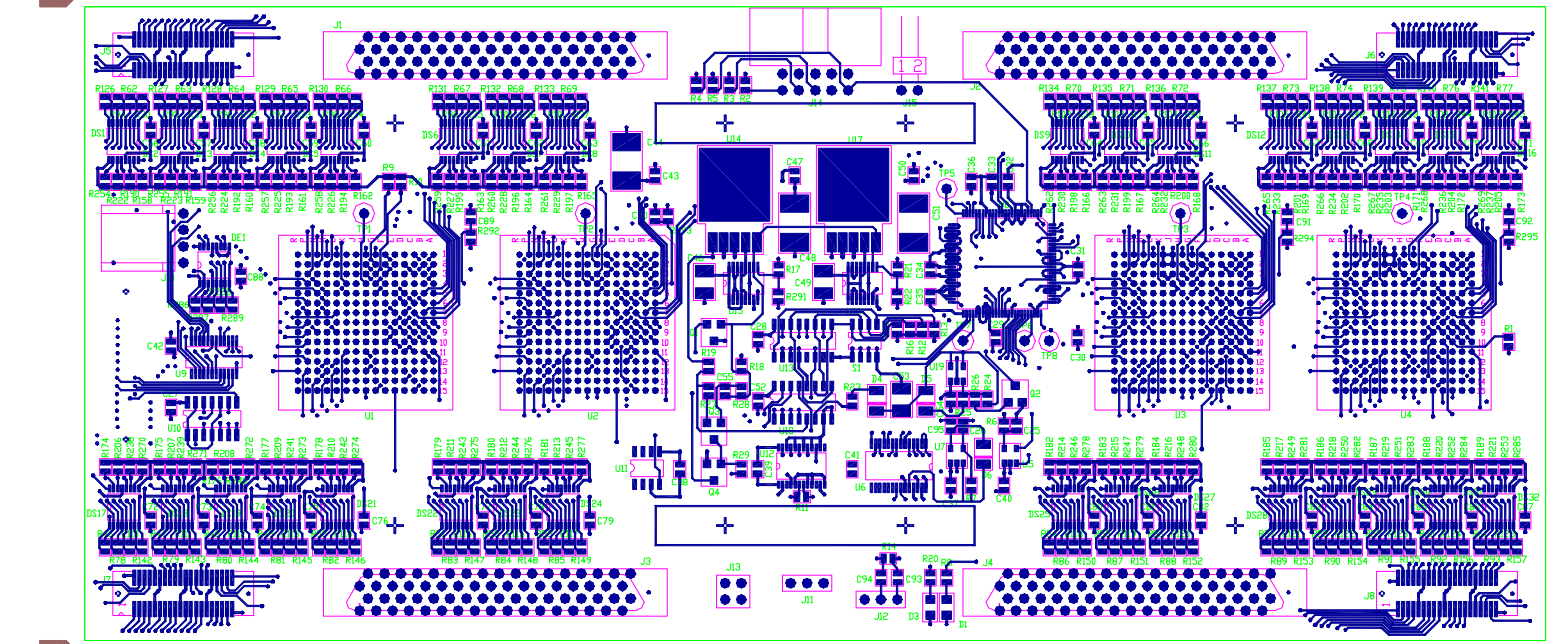

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Why pulsing DTs ?

- Simulate tracks on a single chamber

⇒ Test setup during installation

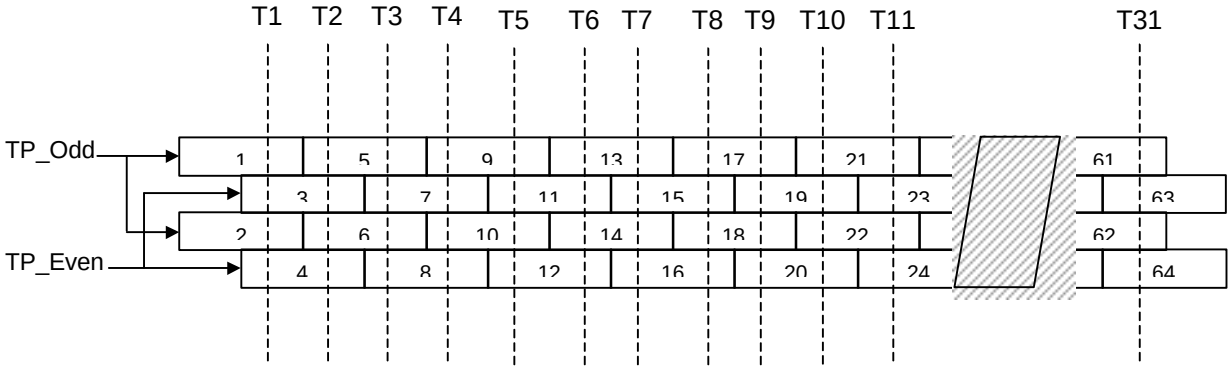
- Test Front End response

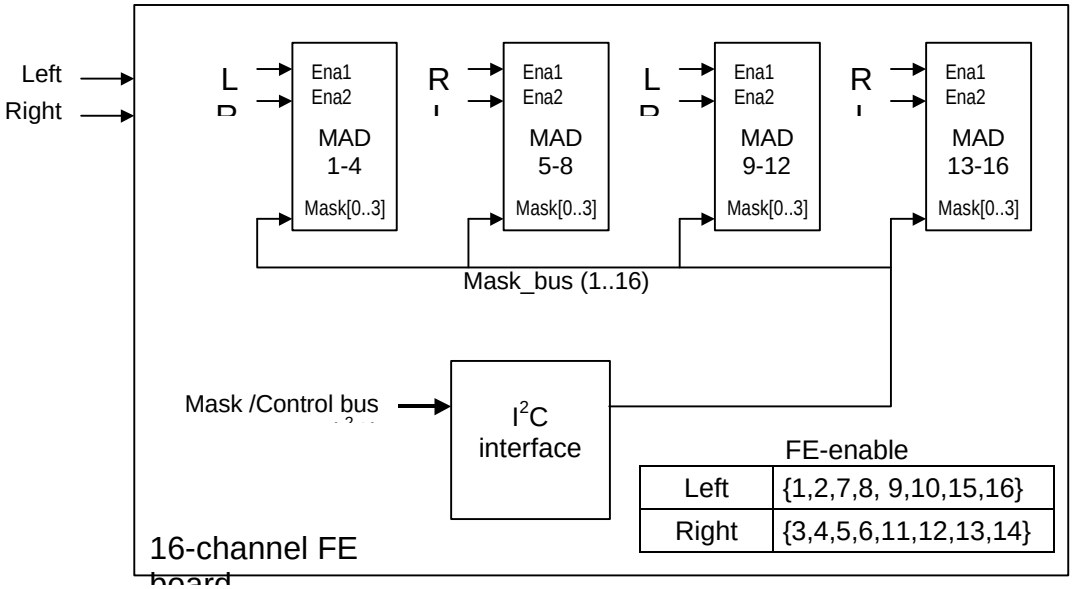
⇒ Special runs

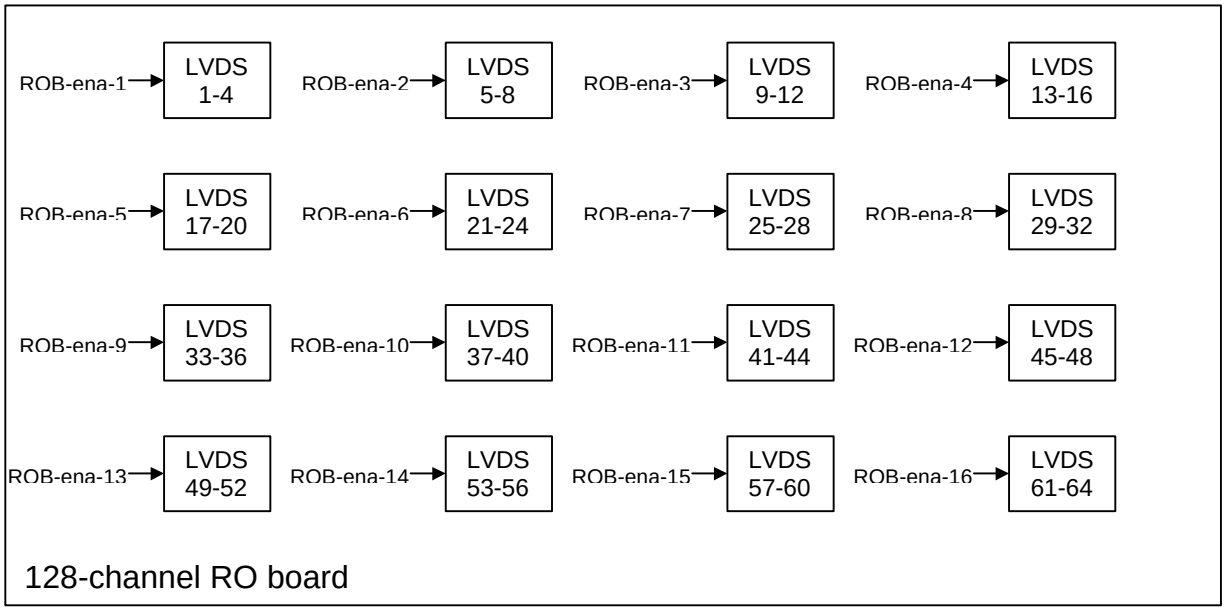
- Monitor readout and trigger synchronization

⇒ Abort gap

Test pulse generation







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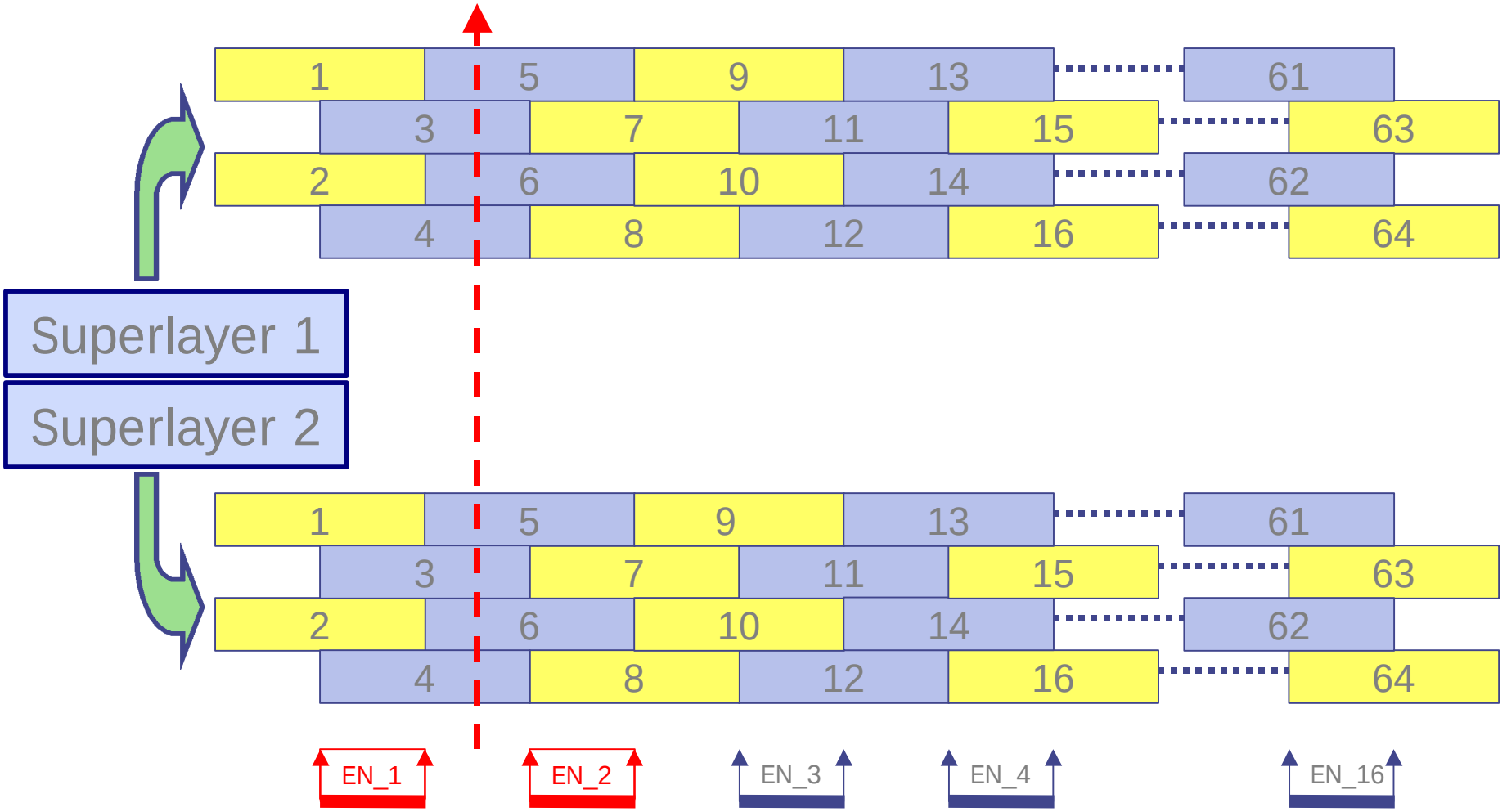
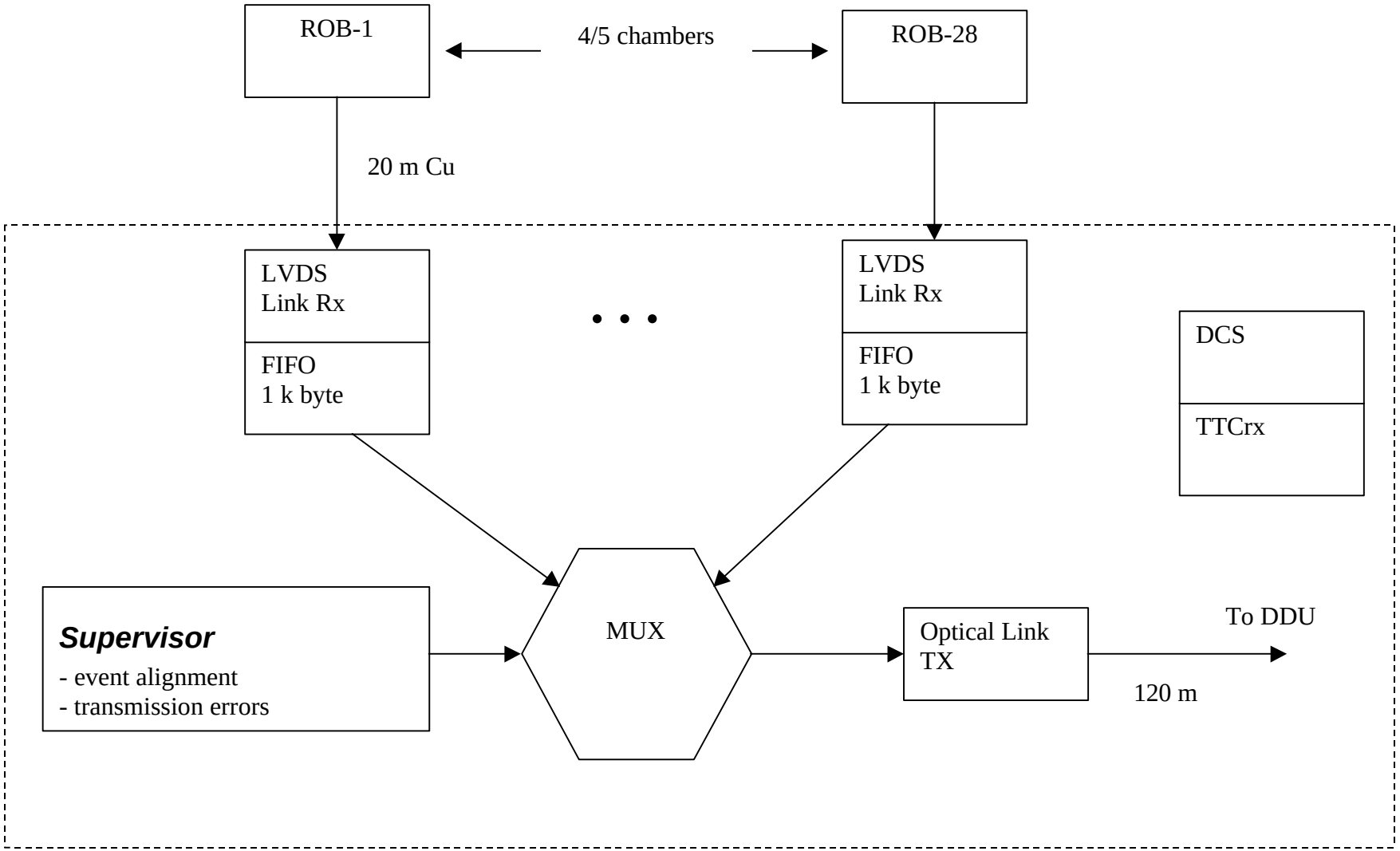
Pulsing a DT chamber:cells 3,4,5,6



DT ROS-Master



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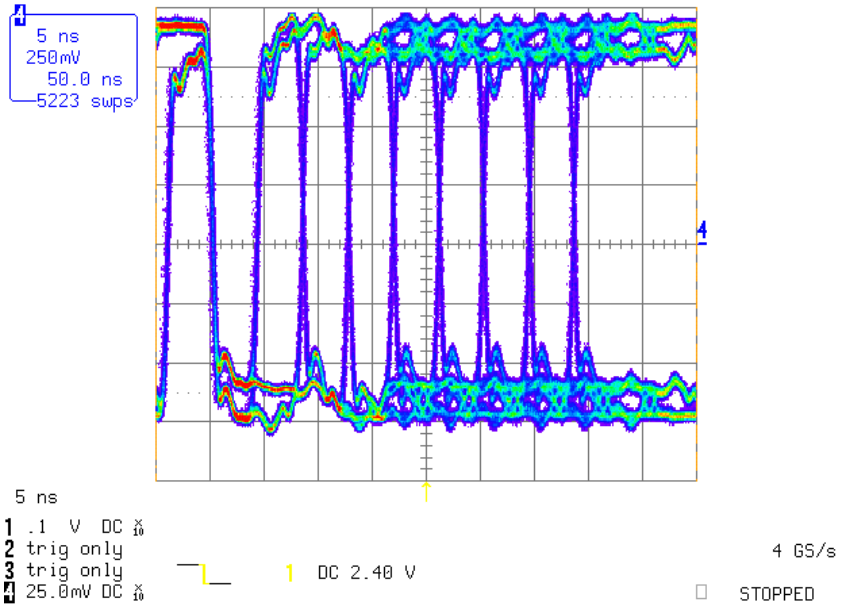
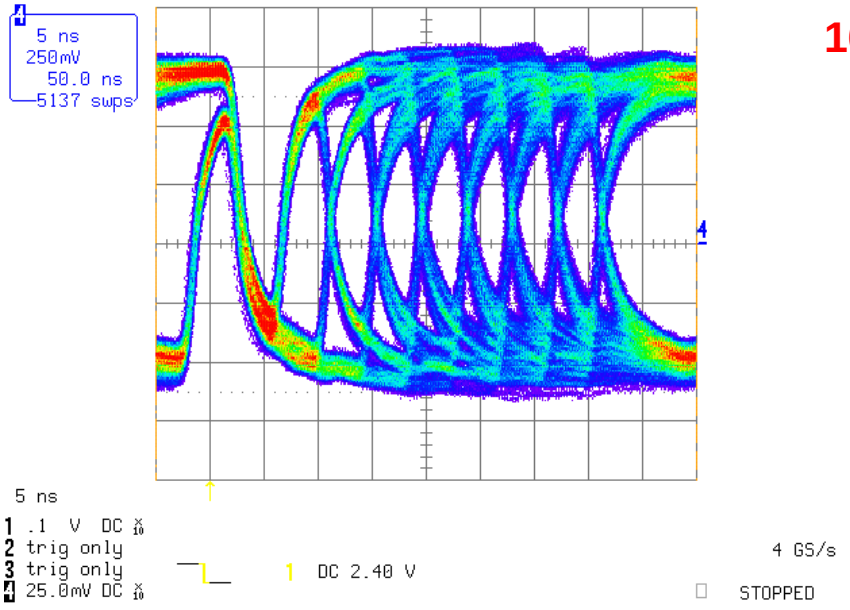
Short cable

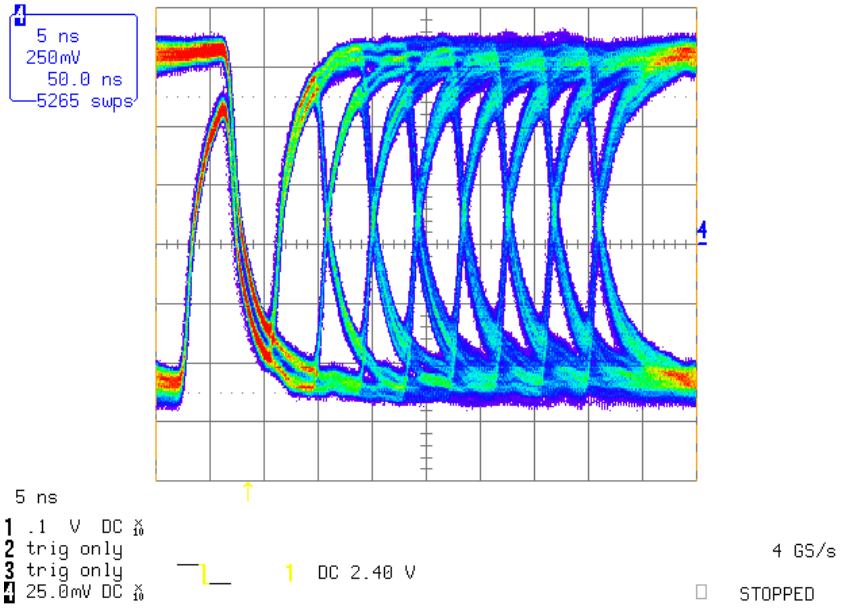


F.B.



16 m

CERN MCX



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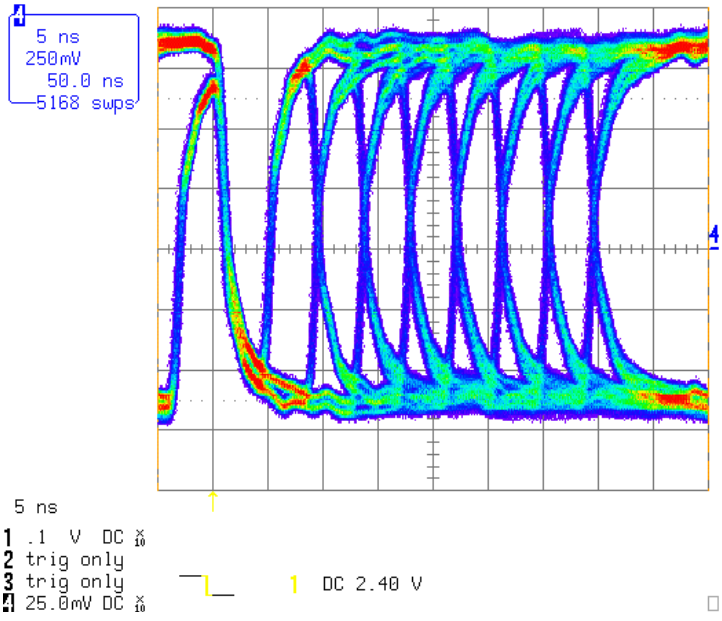
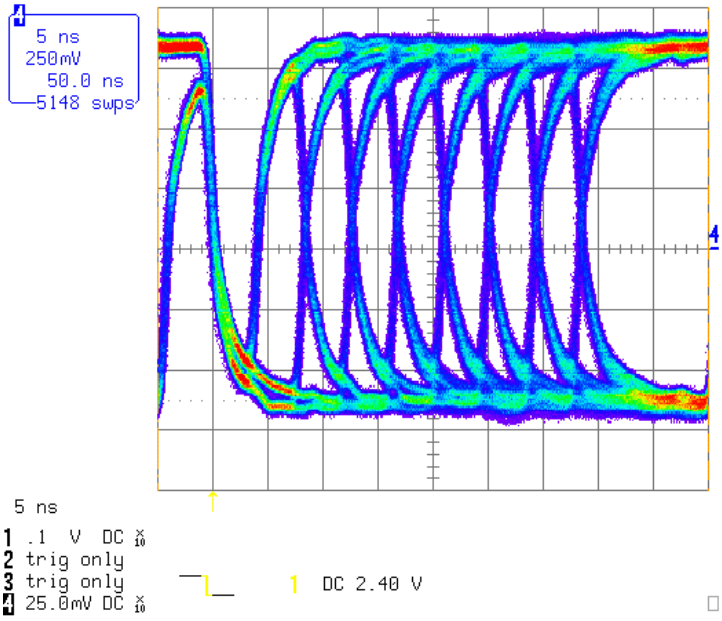
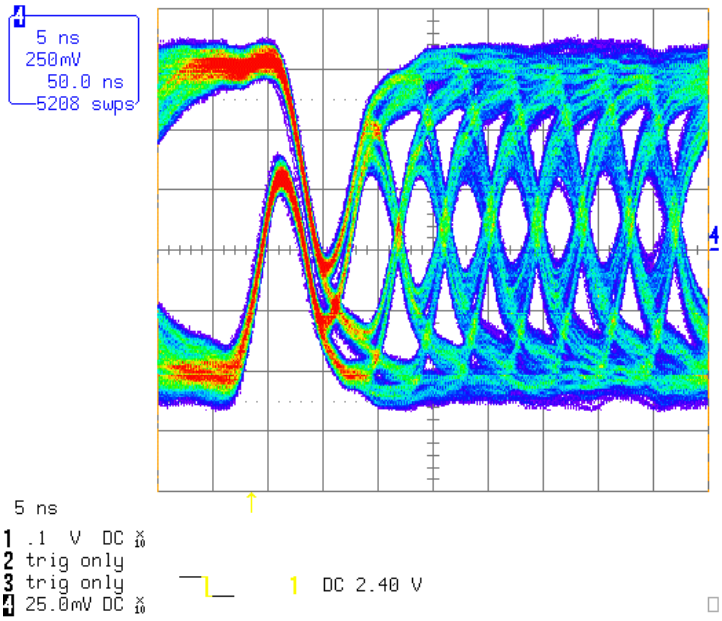
AMP-



BB-



Amphenol-flat-0.635



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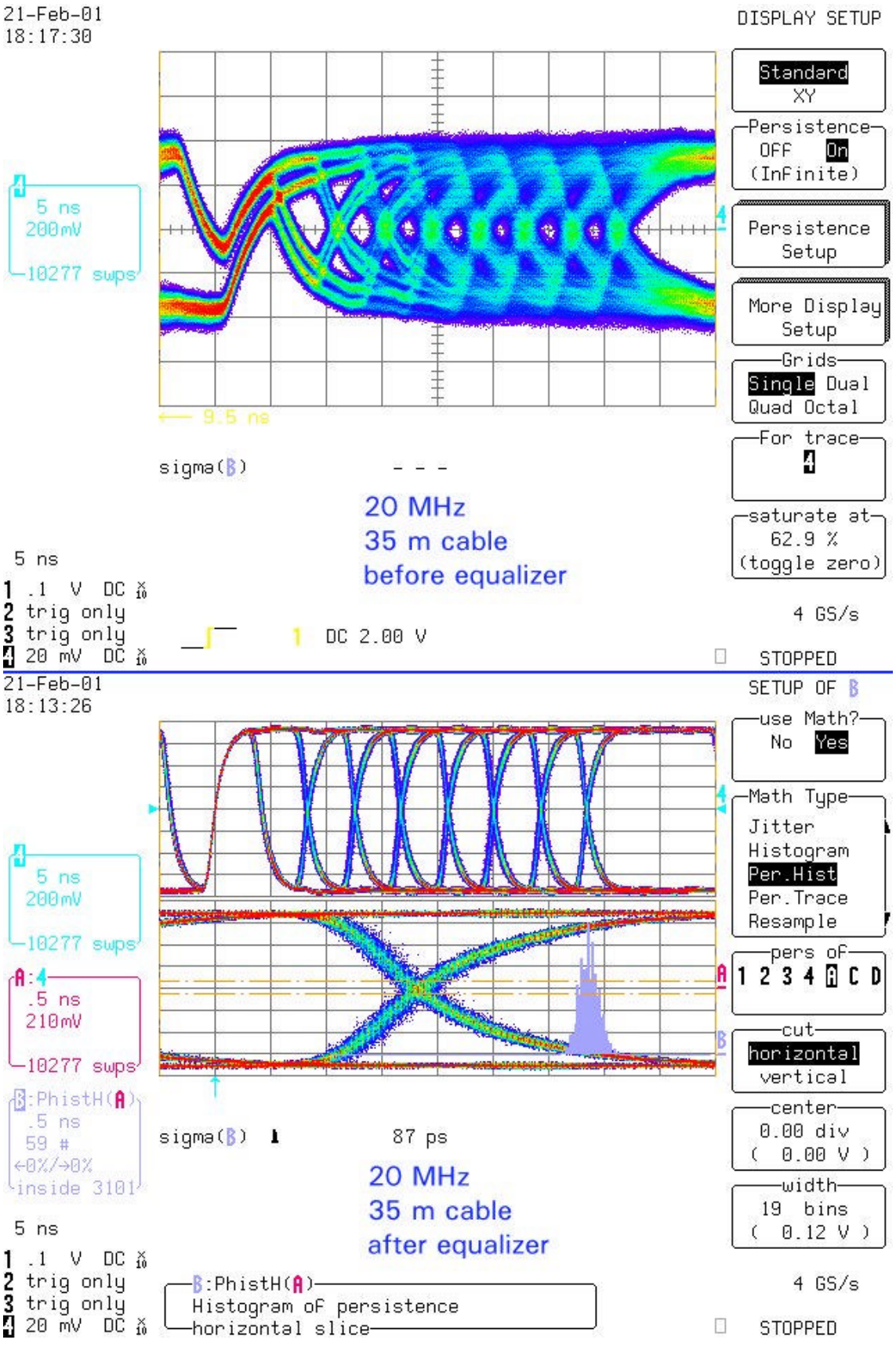
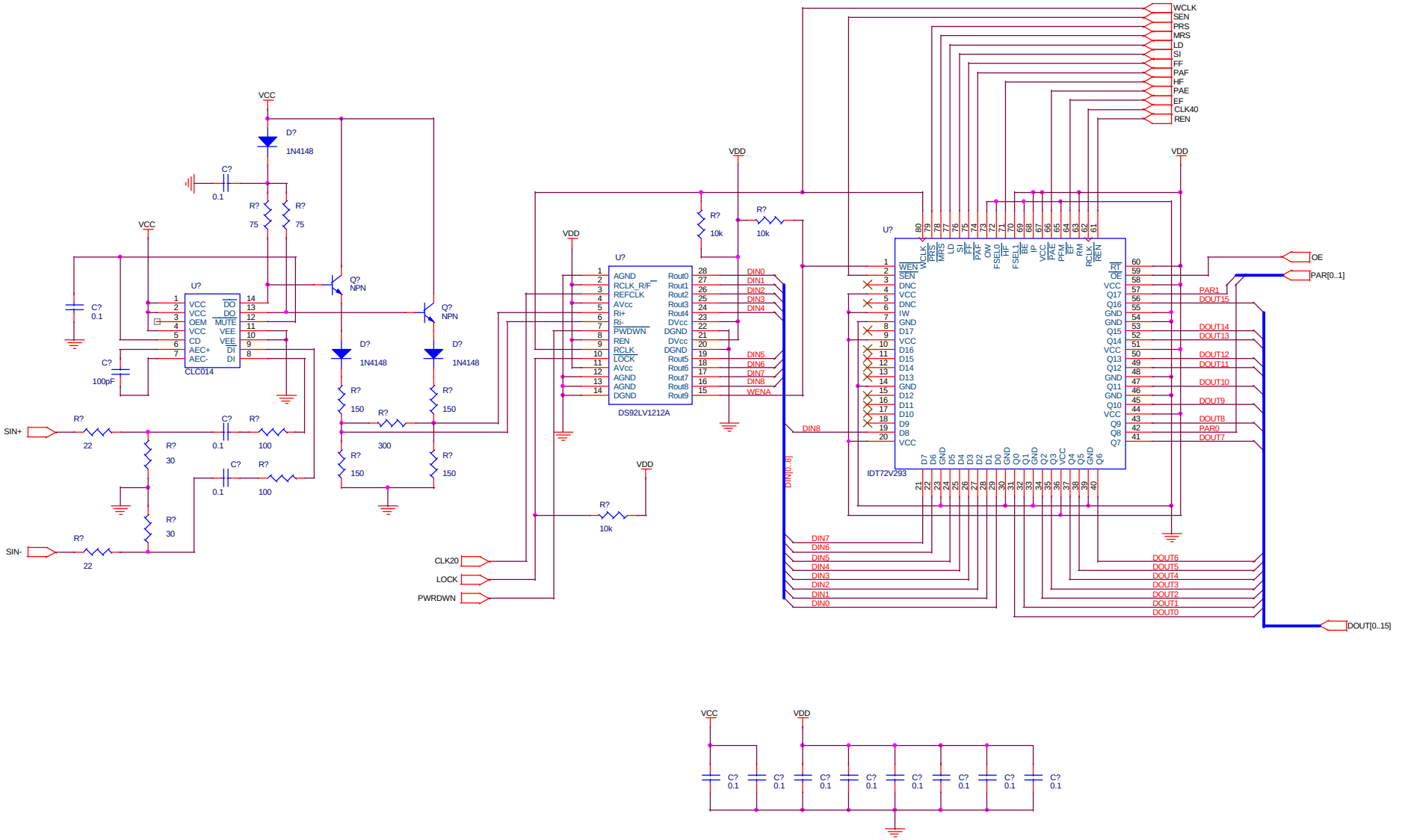

21-Feb-01
18:17:30
DISPLAY SETUP
Standard
XY
Persistence
OFF On
(InFinite)
Persistence
Setup
More Display
Setup
Grids
Single Dual
Quad Octal
For trace
4
saturate at
62.9 %
(toggle zero)
4 5 ns
200mV
10277 swps
9.5 ns
sigma(B) - - -
20 MHz
35 m cable
before equalizer
5 ns
1 .1 V DC
2 trig only
3 trig only
4 20 mV DC
1 DC 2.00 V
4 GS/s
STOPPED
21-Feb-01
18:13:26
SETUP OF B
use Math?
No Yes
Math Type
Jitter
Histogram
Per.Hist
Per.Trace
Resample
pers of
1 2 3 4 A C D
cut
horizontal
vertical
center
0.00 div
(0.00 V)
width
19 bins
(0.12 V)
4 5 ns
200mV
10277 swps
A:4
.5 ns
210mV
10277 swps
B:PhistH(A)
.5 ns
59 #
←0%/→0%
inside 3101
sigma(B) 87 ps
20 MHz
35 m cable
after equalizer
5 ns
1 .1 V DC
2 trig only
3 trig only
4 20 mV DC
B:PhistH(A)
Histogram of persistence
horizontal slice
4 GS/s
STOPPED


VCC
VDD
D?
1N4148
C?
0.1
R?
75
Q?
NPN
U?
CLC014
100pF
SIN+
SIN-
22
30
100
150
300
10k
DS92LV1212A
AGND
RCLK_R/F
REFCLK
AVcc
RI+
RI-
PWDWN
REN
RCLK
LOCK
DGND
DVcc
Rout0
Rout1
Rout2
Rout3
Rout4
Rout5
Rout6
Rout7
Rout8
Rout9
DIN0
DIN1
DIN2
DIN3
DIN4
DIN5
DIN6
DIN7
DIN8
WENA
CLK20
LOCK
PWRDWN
IDT72V293
WCLK
SEN
PRS
MRS
LD
SI
FF
PAF
HF
PAE
EF
CLK40
REN
OE
PAR[0..1]
DOUT[0..15]
DIN[0..8]
PAR1
DOUT15
DOUT14
DOUT13
DOUT12
DOUT11
DOUT10
DOUT9
DOUT8
PAR0
DOUT7
DOUT6
DOUT5
DOUT4
DOUT3
DOUT2
DOUT1
DOUT0

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GOL Reference Maual

http://proj-gol.web.cern.ch/proj-gol/

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Error Monitoring and Actions

HPTDC

- All internal state machines are checked for illegal states
- Memories are continuously checked for parity errors
- DLL locking state is checked at every hit
- JTAG data and programme registers include parity check
- Every output data byte transmitted includes a parity bit

Error status can be monitored through JTAG:

- Vernier error
- Coarse error
- Select error
- L1 buffer error
- Trigger FIFO error
- Matching state error
- Readout state error
- Setup error
- Control error
- JTAG error

Errors that affect a limited number of events are flagged in data stream

I addition, on global error detection HPTDC can be programme to:

- Ignore errors
- Mark subsequent events with special error flag
- Bypass, sets HPTDC into a bypass state in which passes token to next HPTDC putting itself out of the data chain

Error Monitoring and Actions (cont.)

ROS Master

- Check parity errors on input links
- Check event alignment between ROB's

The following cases can be flagged to DDU

- Warning
  - FIFO almost full
- Errors
  - Input link not locked
  - Input link time out
  - Parity error
  - FIFO full
  - Event misalignment

Input links can be automatically masked on error or through DCS

From ROS Master to DDU possibly G-link protocol, allowing for control and data frames, with embedded valid frame check.

The CMS DT Muon DDU: a PMC based interface between frontend and data-acquisition

F.Benotto, F.Bertolino, R.Cirio, G.Dellacasa

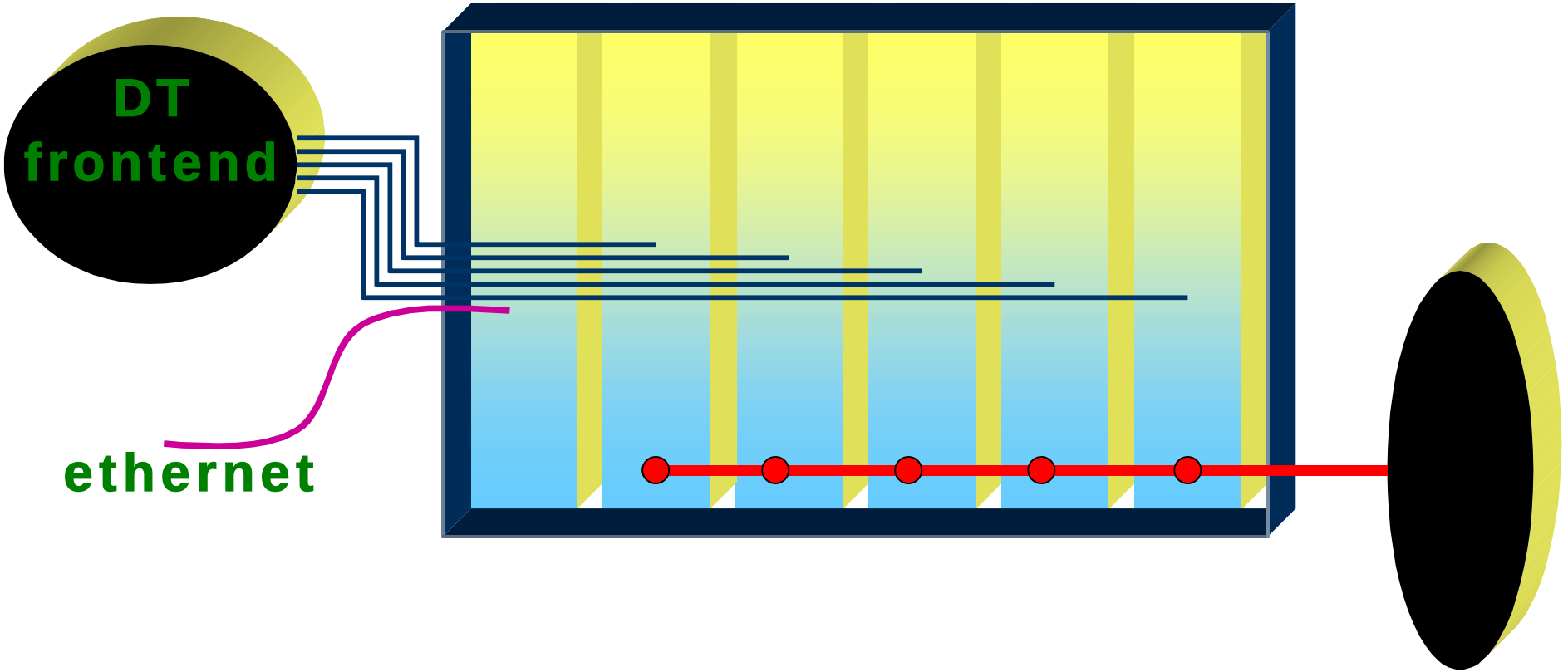
INFN Torino - Italy

May 14, 2001

The DT DDU functionalities

- Get data from frontend
- Check data
  (format,errors,alignement,...)
- Monitor frontend FIFO status
- Format data (8b $\vee$ 32b) for DAS
- Take action in case of warnings/errors
- Allow test/spy

Layout of the DT DDU crate



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The VME DT DDU prototype

- 6U VME form factor
- Cypress Hotlink CY7B933 serial link
- 2k*9-bit input FIFO
- Xilinx XC4005E
- 2 256*18-bit output FIFOs
- VME interface
- built and tested with frontend protos

The PMC DT DDU prototype

- 2 independent input channels featuring:
  - 2* HP optolink HFBR 5208
  - 2* Cypress Hotlink 7B933SC serial link
  - 2* (2k*9b) input FIFO
  - Xilinx XCS40XL FPGA
  - 128k * 36b output FIFO
  - PLX 9080 PCI bridge
- PCB in production

Low Voltage System

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Low Voltage Power Requirements

	DT power consumption (amps)				
		Minicrate		FEB	
	Qty	MC 3.3V	MC 5V	FE 2.5V	FE 5V
Chamber type					
MB1	60	27,2	0,8	3,2	1,6
MB2	60	30,5	0,8	3,6	1,8
MB3	60	35,3	0,8	4,1	2,0
MB4 (1, 2, 3, 5, 6, 7)	30	32,0	0,8	3,8	1,9
MB4 (8, 12)	10	31,8	0,8	3,7	1,8
MB4 (9, 11)	10	17,6	0,8	1,9	1,0
MB4 (4 left)	5	27,0	0,8	2,9	1,4
MB4 (4 rigth)	5	27,0	0,8	2,9	1,4
MB4 (10 left)	5	22,3	0,8	2,4	1,2
MB4 (10 rigth)	5	22,3	0,8	2,4	1,2
Total	A	7529	200	877	438
	W	24845	1000	2192	2192
		30229	**W**		

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Front-End LV PS requirements

+5 V (1 linear supply per chamber)

- voltage output settable between + 4.75 and + 6.25 (to overcome voltage drops due to cables)
- crowbar protection adjustable up to 6.5 V
- output current max 5 A (200 % of required for 1K channels)
- current protection settable in steps of max 0.5 A
- line regulation (220 +- 10 %) < 0.5 %
- load regulation (0 - 100 %) < 0.5 %
- ripple < 5mVpp (20 Hz - 50 MHz)
- temperature coeff. < 0.1%/C
- MAXIMUM ALLOWED OVERSHOOT (load & line transients) < 200mV
- shielding winding between primary and secondary of transformer

+ 2.5 V (1 linear supply per chamber)

- voltage output settable between + 2.5 and +3 (to overcome voltage drops due to cables)
- crowbar protection adjustable up to 4 V
- output current max 10 A (200 % of required for 1K channels)
- current protection settable in steps of max 1 A
- line regulation (220 +- 10 %) < 0.5 %
- load regulation (0 - 100 %) < 0.5 %
- ripple < 5mVpp (20 Hz - 50 MHz)
- temperature coeff. < 0.1%/C
- MAXIMUM ALLOWED OVERSHOOT (load & line transients) < 150mV
- shielding winding between primary and secondary of transformer

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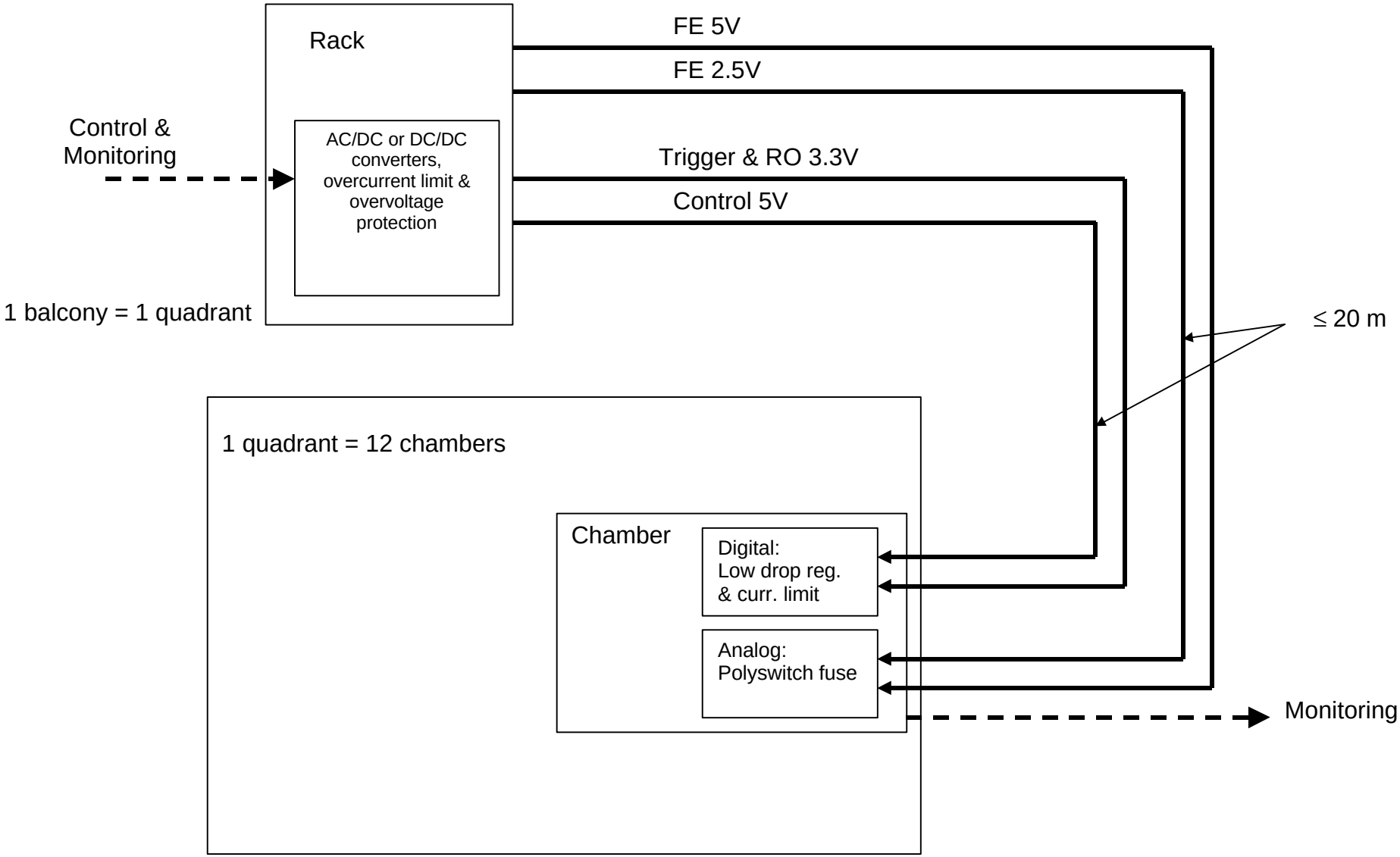
DT Basic LV Distribution



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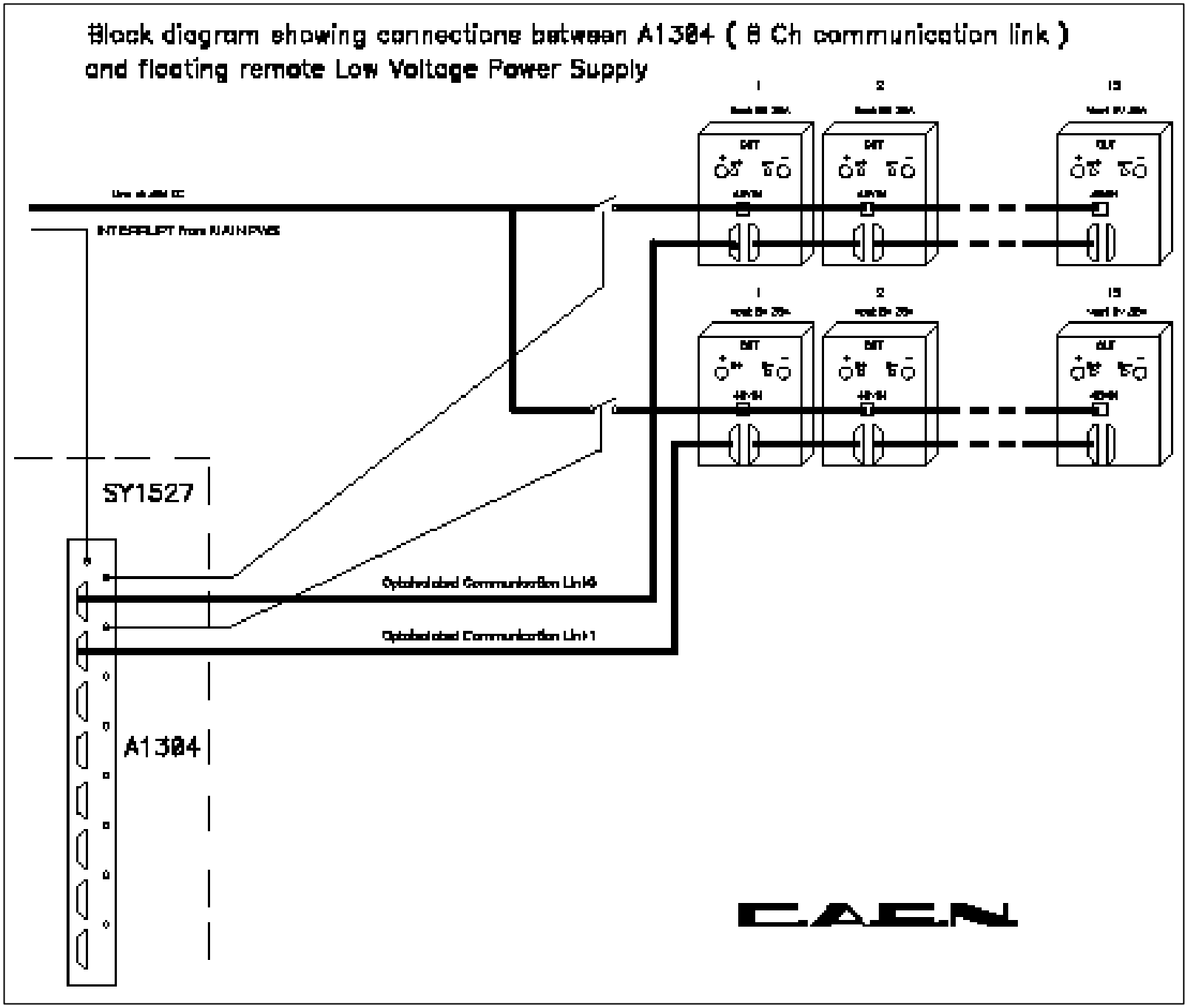
Block diagram showing connections between A1304 (8 Ch communication link)
and floating remote Low Voltage Power Supply
SY1527
A1304
CAEN

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CRISA Developments

In 2000 they built and tested a low noise 5V-4A AC/DC converter with the following main characteristics:

- Input Voltage: 220V / 50 Hz
- Output voltage regulation: 5V $\pm$ 0.5%
- Output voltage ripple < 5 mV pk-pk
- Maximum output current: 4 A
- Overshoot during start-up: < 100 mV
- Input / Output galvanic isolation
- Operation in magnetic field up to 0.1 T

In 2001 they developed a high power DC/DC converters

- Input Voltage: 230 V
- Output voltage: 4 V
- Maximum output current: 40 A
- Operation in magnetic field up to 0.1 T

A LV system is now under study.

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DT sector ground distribution