Electronics Meeting

Padova, December 11-15, 2000

Participants:

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Status

BTI

One BTI module (with 4 BTI's) has been successfully tested with neutrons (< 60 MeV, 10^{12} n/cm^2). No tests done with protons.
1400 dies, from previous prototype production run, should arrive in the next days. They will be used to produce BTI module prototypes.
The order, for the new production run, will be placed to Atmel around December 20.
Five pieces will be delivered in 30 weeks (August). Then, there are only 4 weeks to test them and give approval for full production. Some hardware will be required to perform these tests, but, in principle, the software already exists.
Production will start 38 weeks after order, and will last for 8 weeks. The full production is for 55k pieces.
Note: 1422 BTI's arrived on Jan 9, 822 were sent to Mipot Jan 11.

BTI modules

Market survey is already done: there are 10 offers.
Tender for production will take 30 weeks. Part of this tender could be the production of module prototypes (?). A BTI module socket for tests will be required.
Meanwhile, 200 pieces (for 800 BTI's) have been submitted to Mipot. First 30 will arrive in 3 months (March), the rest in 7 months.

Traco

Atmel refuses to continue with this project. A new foundry is required. A cross library has to be produced. This may take only 2 weeks. The simulation may be much more complicated, from a few weeks to infinite time: this task consists of running a simulation with test vectors (already existing) and to compare results with previous simulations (Atmel library). In case of mismatch, to find the problem could be very difficult.
The question is, to witch technology migrate? Alcatel seems to be a good choice (0.5 um). Another possibility would be IBM (0.25 um) for witch a tender has already been done (CERN). A serious constraint to adopt this last technology is that it would require an additional power regulator on TRB, and the board is already too crowded.

Meng Guang and Marco Bellato are evaluating libraries in 0.5-0.35 um technology available trough Europractice.
One important point is that this design is at gate level (not HDL).

Marco Dallavalle points out that “in the chip currently available, loading of the LUTs is only possible through Parallel Interface; LUTs cannot be loaded via JTAG. All other configuration operations can be done via both routes, providing a robust environment; failing in loading the LUTs at the beginning of a running period means the chamber is dead for the trigger”.
Also, what exists “is a first prototype with partial functionality (only inputs from one superlayer are functional, which means correlation cannot be tested)”.

TRB

Prototypes for both (phi, theta) exist with minor faults to be corrected in the next prototype version. Only some critical components of the board have been tested successfully with neutrons.

CCB & SB

This is a set of two boards. The control functionality is place in CCB and on one side of SB. TSM design is placed on the other side of SB.
A first prototype exists. Tested with neutrons. RAM’s did not pass the test. A list of tested components can be fount at http://marcodv.home.cern.ch/marcodv/TSM.html
Operates correctly with TRB. Still needs to be tested with respect to FE and RO.

Minicrate

At the moment only a draft design exists.

List of things to do

BTI

In order to validate production chips we need a jig. This jig should be tested beforehand with existing BTI chips: the package is in fact the same as the new ones.
Radiation test should be performed on first (5) prototypes to be delivered in August 2001. However, it seems very unlikely to be able to perform radiation tests in such a short period.

BTI modules

Test 30 pieces coming in March-April with existing socket prototype and board. Prepare new socket, adequate for burn-in tests, and new board. They need also a new test procedure (quicker and with a wider faults coverage). New software should be written.

TRACO

First we need to decide on the new technology (or go for a tender). Once the technology is decided we can start with library translation followed by simulation.

Flavio Dal Corso et al. say “concerning the proposal to modify the TRACO following the suggestion of Marco Dallavalle, Meng Guang and Marco Bellato are trying to build a cross library, without understanding the details of the TRACO. If a significant change

has to be done in the TRACO it should be clear that it would require a much longer time. A decision on this point should be taken immediately".

For the validation of the prototypes a test procedure has to be defined. It needs essentially a TRB, a CCB, the Pattern Unit from INFN-Bo, and software.
TRACO has to be tested with neutrons, and in particular LUT's which are actually RAM.

TRB

Both boards (theta and phi) need a 2nd prototype: fix clock lines, TRACO and TSS pinout, and other minor changes.
Decide on pig-tail connectors based on cost, available space, reliability, etc.
Aging tests to be performed on prototypes and during production.
A jig will be required to test boards in the Lab: to check production.
30-channel TRB is completely missing. Dimensions are already fixed.
The TRB suffer the same alignment problem on the AMP connector, as the CCB (see below).
The board should be re-tested with neutrons after changes.

CCB & SB

A new (improved) partitioning is required.
TSM design has to be merged with control functions on SB.
The possibility to implement two control boards (or duplicate some control functions) in a minicrate should be studied to improve reliability.
In the analog part, fast enable control signal must be changed from PECL to LVDS.
Also rise time of I2C signals should be adjusted to reduce noise on FEB. Threshold levels need to be checked.
Test operation with ROB's is required.
Radiation tests with neutrons/protons must be completed: in particular for those components that failed during previous test, like memory chips, etc.
Aging test of full board: 2000 h.
Software: to be done almost from scratch.
AMP connectors show alignment problems. Two options: check with pick & place company and look for replacement connector.
RO bus termination board: to be studied.
Present CCB does not have TTC. To be checked with next version.

Link board

Final prototype is done, but not completely decided where/how to put the connectors.
The overall space available is 9 cm.

Minicrate

One mechanical minicrate prototype will be built and tested beginning of 2001.
This minicrate will be equipped with cabling and dummy boards for thermal tests.
When available real boards will replace dummy ones.
A test jig must be built to check minicrates coming out of assembly factory.

Trigger links

It has been agreed that 2 low order bits are for bx counter and there is another bit for control/synchronization.
There are serial copper links from chambers to balconies (Sector Collector) and optical links from balconies to Track Finder. The tests of the serial copper link needs a new test jig.
In each sector there is 1 optical link per phi view and 2 links for the 3 theta views. In total 6 links per Sector.

We discussed the use of the CERN opto-link serialiser, and the preliminary conclusion was that it would simplify the readout. Peter Sharp later checked with Sandro Marchioro that the chip had the performance we assumed, which he confirmed.

Synchronization

This procedure is for chambers already installed in the wheel. Full RO must be operational.

Clock phase

Beam on.
BTI set to minimum acceptance. Set drift velocity to an approximate value.
Trigger set in special mode for synchronization: trigger on any data from BTI.
Look for HQ trigger rates as function of clock phase: max rate at the correct phase. Set clock phase
Adjust drift velocity to optimize efficiency.
Iterate a few times.

It is also possible to do this adjustment using mean timers.

Synchronize bx number on TTC

Histogram HQ triggers at CCB.
Read out histogram through DCS.
Compare with bunch pattern.
Adjust bx counter on TTCRx.

Trigger links

Track Finder resynchronize inputs for all sectors.