Overview of the Read-Out System for the CMS Drift Tube Chambers.

C. Fernández-Bedoya, J. Marin, J.C. Oller, C. Willmott

Lab. Electrónica y Automática. CIEMAT.
Avda. Complutense, 22. 28040 – Madrid. SPAIN.
Cristina.fernandez@ciemat.es

Abstract

The final architecture of the read-out system for the CMS drift tube chambers is presented. It is staged in two levels: firstly, the Read Out Boards (ROB), responsible for the time digitalization of the incoming signals from the front-end electronics related to Level 1 Accept trigger; and a second level, the Read Out Server boards (ROS), for merging data from ROB´s and transmitting the information out of the cavern to the DAQ system interface (DDU/FED).

The chosen architecture, as well as the link bandwidths, failure detection and power supply protection circuitry, etc, fulfil the experiment requirements of trigger and hit rate, radiation tolerance, limited supervision and power consumption, among others.

I. INTRODUCTION

The electronics of the read-out system of the CMS drift tube chambers (DT´s) [4] is responsible for the time digitalization and data transmission of the signals generated in the drift chambers to higher levels of the DAQ system.

One of the most important features of CMS is its precise and efficient muon detection capability which takes place thanks to three different types of detectors [1]: RPC´s (Resistive Plate Chambers), CSC (Cathode Strip Chambers), and DT´s. These last ones are located on four concentric layers along the beam line inside the five wheels of the iron yoke of the CMS barrel.

There is a total amount of 250 DT chambers, each of them consisting in three superlayers, for both Φ and θ coordinate measurement, attached to a structural honeycomb support. A superlayer is made up of four layers of drift cells, and the total amount of cells in the detector is 172,200 channels.

Any charged particle track going through a cell volume will generate a signal in its anodic wire that will be processed by the front-end electronics located inside the chamber gas enclosure. The time measurement performed by the read-out electronics of the discriminated signal will allow the later reconstruction of the particle tracks and further momentum measurement.

The time digitalization of the signals is performed at the ROB´s, located in the so-called minicrate together with the DT muon trigger electronics. This minicrate is an aluminium box that will be attached to the honeycomb of the chambers.

Two FTP cables will be used for sending digitalized data from each minicrate to the 30 meters far away rack in a towers on one side of the CMS wheels where the ROS boards will be located. Each ROS will merge data from one sector of the chambers through a 100 m. optical link to the DDU´s in the USC55 control room. Accordingly, their main task will be the multiplexation of 1500 copper links into 60 optical links.

A. System requirements

The developed system is expected to be operated under certain constraints, as it is the high frequency of triggers expected (100KHz) due to the high luminosity of the LHC, which will generate a large amount of data that requires a fast processing system. The charged particle rate expected at the barrel is about 10 Hz/cm^2, which will be reduced to 1 Hz/cm^2 of muons by the Level 1 trigger system [2], providing 1 KHz of hits per channel, and a occupancy of 0.76% in the whole detector.

As the L1 trigger latency is 3.2 μs, memories have to be large enough to store hits until matching can be done. On the other hand, as the maximum drift time (400 ns) is much larger than the bunch crossing period (25 ns), a mechanism that deals with overlapping triggers is required.

Moreover, a remnant radiation is expected in the detector area as a result of the products of the successive interactions. This forces the employment of radiation tolerant devices that will have to be tested. The neutron fluence expected in 10 years of operation is of 10^{10}cm^{-2}, being the charged particles flux of 10 cm^{-2}s^{-1} and the integrated dose of 1 Gy [1].

Besides that, the high magnetic fields created by the solenoid impose certain restrictions to the electronics mainly to the power supplies and cooling systems. For example, the allowable power dissipated at the tower racks is limited to the rack cooling provided by tangential fans. On the other hands, minicrates are water cooled to avoid any heat transfer to chambers.

The operation of the CMS detector is foreseen to last about 10 years and during this time, the maintenance may be possibly restricted, and in particular the electronics located inside the detector wheel. Therefore, a robust and reliable system is demanded, requiring the less intervention as possible.

The read-out system has been developed according to these requirements and it is being tested to guarantee its performance.

II. READ-OUT BOARDS (ROB)

Read-Out Boards are built around a 32-channel high performance TDC, the HPTDC, which is the 3rd generation of TDC´s developed by CERN/EP Microelectronics group [3, 9], and it has been implemented in IBM 0.25 μm CMOS technology.

A. HPTDC (High Performance Time to Digital Converter)

This highly programmable TDC is based on the Delay Locked Loop (DLL) principle, providing a time bin of 25/32ns = 0.78 ns, that is, 265 ps resolution, when it is clocked at the LHC 40.08 MHz frequency. This time resolution is enough for the 1 ns required to obtain a single wire resolution of 300 μm in the position measurement. Higher resolution modes are available thanks to an internal PLL and possible interpolation using 4 channels, up to 25 ps.

As it can be seen in the figure 1, the digitalized signals from each of the 32 channels are first stored in the input "hit registers" and then are driven to the 256 words deep group memories common to every 8 channels (Level 1 buffers). The output of these group memories is merged into a common 256 deep read-out memory after the trigger matching is performed. Until this operation can be done, the arriving triggers are stored in a 16 deep FIFO. Besides its complexity, matching is done in a rather fast way, selecting from memory hits within a programmable time window. Accordingly, hits coming from the chamber channels are related to a common trigger allowing correlation of particle tracks to the event where they were generated.

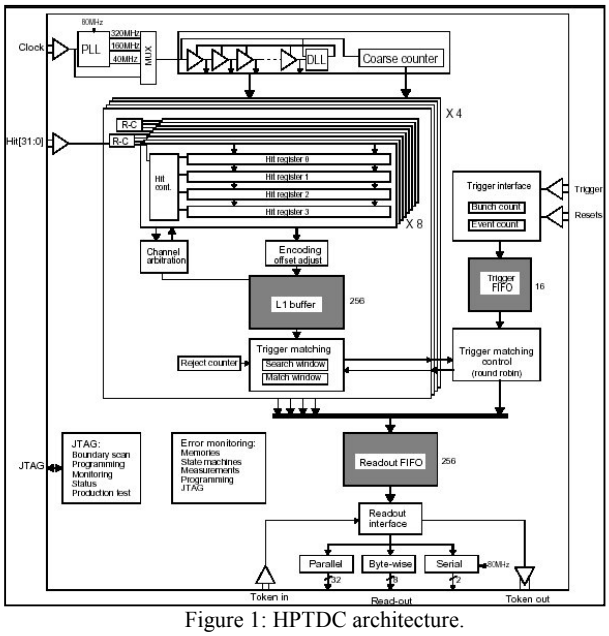

Figure 1: HPTDC architecture.

Also, in this HPTDC, an effective reject mechanism allows overlapping trigger handling. It has been designed to stand hit rates up to 2 MHz hit rates, much more than our needs as noisy channels will be of tens of KHz, and it also stands up to 1 MHz trigger rates.

The HPTDC has been implemented in a radiation tolerant technology, standing up to levels of 30 Krad total dose with slight increase in power consumption.

Other remarkable features of this TDC are the JTAG programming interface, a flexible signal interface and readout modes, etc. It also has internal counters for the event identification count and for the bunch crossing identification count. This information can be attached to the output data with each event, as well as programmable headers and trailers, error flags and debugging information.

B. ROB Architecture Description

The number of HPTDC´s per ROB has been decided following a compromise between the number of unused channels when the granularity is too small and the multiplication of common components when it is too big.

Finally, each ROB has 4 HPTDC´s connected in a clock synchronous token ring passing scheme, where one of them is configured as master to control the token of the read-out data chain. The token ring scheme is designed following a failsafe mechanism (Fig. 2), trying to avoid that failure in one of the TDC´s interrupts the whole ROB operation. A hardware and also a software bypassing system has been implemented.

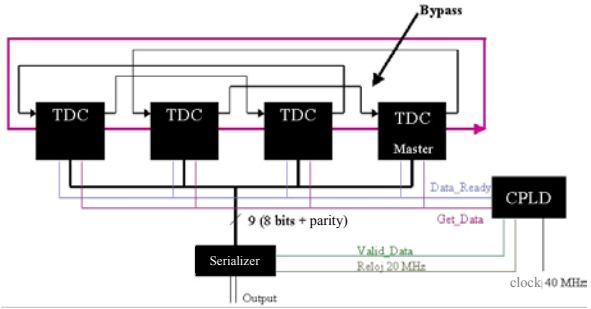

Fig. 2: Diagram of the token ring connection of HPTDC´s on ROB.

When the read out is performed, the HPTDC having the token drives its data in a byte-wise mode (8 bits in parallel out of the 32 bits per word) into a LVDS link serializer. An Altera MAX7000 CPLD manages the data_ready/get_data protocol, slowing down the readout frequency to 20 MHz.

This CPLD also manages the channels enabling mechanism for testing chambers during spill interleaves, simulating artificial tracks.

On the Altera CPLD registers a triple redundancy mechanism that solves 1 bit upsets has been implemented, and also a single event upset counter for radiation tests.

Every trigger will generate one ROB event block, with a master header and trailer that includes information of the bunch and event number and number of words transmitted,

and with the time measurement words, which include information about the channel and HPTDC number that received the wire signal.

For the average rate expected in CMS that will mean a throughput of 16 Mbps, much less than the maximum 200 Mbps of the serializer. The BER measured in these 30 m link between ROB and ROS was less than 10^{-15}.

The JTAG interface for TDC programming and monitoring is included in a parallel bus shared by every ROB in a minicrate (ROBUS). This bus also carries among others: trigger signal, event reset, bunch reset and other test pulse control signalling. Independent point to point connections are used to minimise interference effects.

Both 2.5V and 3.3V power supply lines on boards are connected to a protection circuitry that in case of 2.5V current consumption over 1.5 A, or 3.3V over 1 A, power supply is disconnected, with powering up cycles every 700 ms.

In figure 3 the different connections of the ROB are showed.

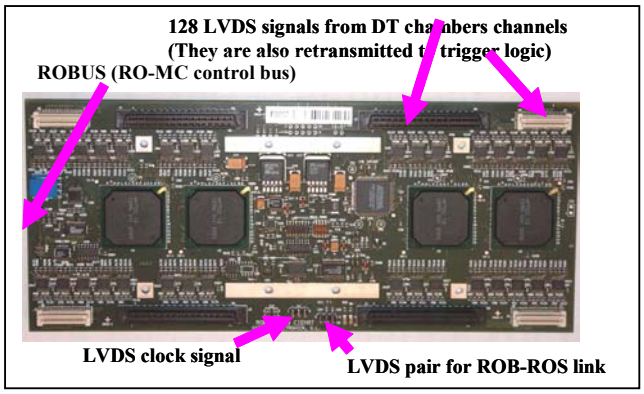

Fig. 3: ROB picture with its connections indicated.

C. Validation tests to the ROB

Several tests have been performed to the ROB´s in order to validate its design and functionality and guarantee its operation in CMS environmental conditions [7].

A 265 ps time resolution has been proved with a crosstalk between one channel and the other 32 neighbours below 350 ps.

Some irradiation tests have been performed at the Cyclotron Research Centre (UCL) with a total fluence of 5.10^{10} protons cm^{-2} at 60 MeV. The results obtained indicate that the mean time between failures (MBTF) of the HTPC is of 3.8 days in the whole detector and 3.4 days for the Altera CPLD.

Two test beams have taken place at the Gamma Irradiation Facility at CERN (GIF) [5], the first one in October 2001 [6], where the ROB functionality was tested, and the other in May 2003 with a whole minicrate connected to a chamber. Both testbeams included 25 ns structured beam and in both of them no errors where found. It was verified that HPTDC can stand high hit rates, and that noisy channels (~ MHz) affect only one group of 8 channels.

Temperature cycles have been performed to the ROB and it has been found a time measurement shift about 14 ps/ºC, with maximum variations of 40 ps/ºC. Voltage variations at regulators outputs are very small (5 mV/30ºC) as well as 2.5V current variations (0.4 mA/ºC).

On the other hand, a lifetime test has been done with one ROB fully operational at an ambient temperature of 105ºC during 4 months and no wrong operation has been found.

D. Minicrate

Depending on the chamber type, the number of channels is different and accordingly, the number of ROB´s per minicrate. The smaller minicrate has 3 ROB´s and the biggest has 7. They are all connected through the ROBUS to the Control Board (CCB) that manages, among others, the TTC signaling. As it can be seen in figure 4, Trigger Boards (TRB) are also located inside the minicrate and connected to the ROB´s to receive TTL translated hit signals.

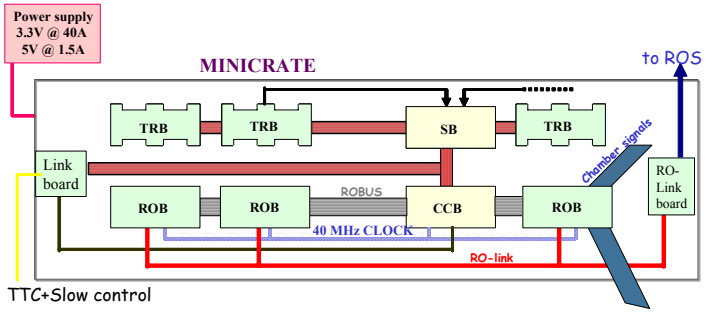

Fig. 4: Diagram of the read-out and trigger electronics located inside a minicrate.

A smaller ROB is also needed for the MB1 minicrate, the ROB-32. Its functionality is the same as the other but it only has one HPTDC, that is, 32 channels.

III. Read Out Server Boards (ROS)

Located in the barrel tower racks there will be 60 ROS boards, 12 per wheel, 1 per sector (four to five minicrates), so each ROS will receive 25 channels of the LVDS copper ROB-ROS link.

This 9U boards will have to multiplex data coming from the ROB´s, adding necessary information of ROB number, link status, etc. and send them to the DDU through a fast link. The GOL serializer developed by the CERN/EP Microelectronics group [8] is going to be used in an 8B/10B Ethernet slow mode (800 Mbps maximum bandwidth).

This ASIC will drive a Honeywell VCSEL transmitting at 850 nm on a multimode 62.5/125 µm fiber. The estimated throughput for the expected data rate is about 270 Mbps, well below maximum bandwidth of the link.

Another feature of this ROS board, is that it also includes a power supply protection circuitry, and a 1 MB memory for testing and data flow snapshots for traceability in case of transmission errors.

A. ROS Architecture

In figure 5 it can be seen how the 25 channels are splitted in seven groups each of them controlled by a CPLD that manages FIFO readout and performs a pooling search for the next event to be read. These CPLD´s are connected in a token ring scheme controlled by an FPGA, that also controls transmission through the GOL serializer. Accordingly, the FPGA indicates the event number to be transmitted and each CPLD fetches it on its FIFO´s in a parallel way, fastening the read-out process.

Besides that, ROS can accept trigger data from neighbour Trigger Sector Collector through a common backplane for testing and synchronization purposes.

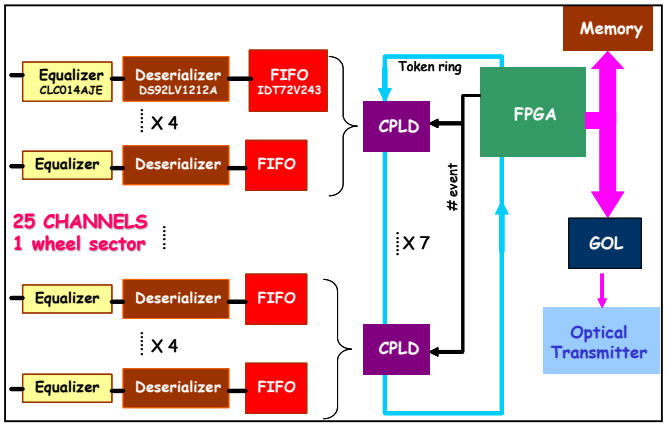

Fig. 5: Scheme of the ROS architecture.

B. ROS-8 prototype

A 6U-VME prototype with 8 channels has already been developed and successfully tested (Fig. 6). It was designed to allow flexible read-out: directly from FIFO´s through VME, from the memory after data format modification and through an Ethernet 800 Mbps copper link (TLK1501).

It consists on 16 kbytes FIFO´s per channel read by a unique CPLD. Data format is changed in a fast way to spend no more than one clock cycle in each word while including all the necessary information.

Fig. 6: ROS-8 prototype.

B. Validation tests to the ROS

Two different tests have been performed with the ROS-8 prototype. Firstly, an irradiation test in UCL with 5 10^{10}cm^{-2} 60 MeV protons where the results obtained are presented in table 1.

Table 1: Mean Time Between Failures for the following irradiated components due to SEU.

	MTBF
Equalizer (CLC014AJE)	17.2 days
Serializer (DS92LV1212A)	2.3 days
FIFO´s (IDT72V263)	2.27 days

Secondly, at the May 2003 GIF test beam, where the ROS-8 was operated to receive data from a whole minicrate, reading data in VME mode. The results were very satisfactory and no error was found.

IV. Conclusions

The final architecture of the read-out system for the CMS drift tube chambers has been presented. The chosen architecture fulfils the experiment requirements of trigger and hit rate, radiation tolerance, limited maintenance and power consumption among others.

After the extensive set of tests performed to the ROB´s, and its success on them, we conclude that the ROB design is ready for production, with the guarantee that it will meet every requirement needed to operate in the CMS detector.

ROS design is still under development, but final architecture has already been defined, and a 25 channel prototype will be built in a short period of time. Experiences with the ROS-8 prototype will allow us confidence on radiation tolerance of the tested devices and its behaviour on data rate conditions similar to the ones that will be found in the LHC.

V. References

[1] CMS. The Muon Project. Technical Design Report. CERN/LHCC 97-32. December 1997.

[2] CMS. The TriDAS Project. Technical Design Report. Volume I. The Trigger Systems. CERN/LHCC 2000-38. December 2000.

[3] High Performance Time to Digital Converter. Version 2.1. J. Christiansen. CERN/EP-MIC. July 2002.

[4] CMS. The Compact Muon Solenoid. Technical Proposal. CERN/LHCC 94-38. December 1994.

[5] "A facility for the test of large area muon chambers at high rates." Agosteo, S ; Altieri, S ; Belli, G ; Bonifas, A ; Carabelli, V ; Gatignon, L ; Hessey, N P ; Maggi, M ; Peigneux, J P ; Reithler, H ; Silari, M ; Vitulo, P ; Wegner, M . Nuclear Instrumentation and Methods. Phys. Res., A : 452 (2000) no.1-2, pp.94-104

[6] "Test Beam Analysis of the First CMS MB2 Drift Tube Muon Chamber." M. Cerrada, N. Colino, B. DelaCruz, C. Fernandez, M.C. Fouz, I. Josa, J. Puerta, L. Romero, C. Willmott, J. Fernandez de Troconiz, I. Jimenez, C. Autermann, K. Hoepfner, H. Reithler. CMS-NOTE-2003-007. 30 April 2003.

[7] "Design and Performance Testing of the Read-Out Boards for the CMS-DT Chambers." C. Fernández, J. Alberdi, J. Marin, J.C. Oller, C. Willmott. Proceedings of the 8th Workshop on Electronics for the LHC Experiments (LECC 2002), Colmar, France, September 9-13, 2002.

[8] "A Radiation Tolerant Gigabit Serializer for LHC Data Transmission." P.Moreira, G. Cervelli, J. Christiansen, F. Faccio, A. Kluge, A. Marchioro, T. Toifl, J.P.Cachemiche, M. Menouni. Proceedings of the 7th Workshop on Electronics for LHC Experiments (LEB 2001). September 10-14, 2001. Stockholm, Sweden.

[9] " A data driven high performance Time to Digital Converter." J. Christiansen, A. Marchioro, P. Moreira, M. Mota, V. Ryjov, S. Debieux. Proceedings of the 6th Workshop on Electronics for LHC Experiments. Krakow, Poland. September 11-15, 2000.