ROB performance in a high luminosity scenario

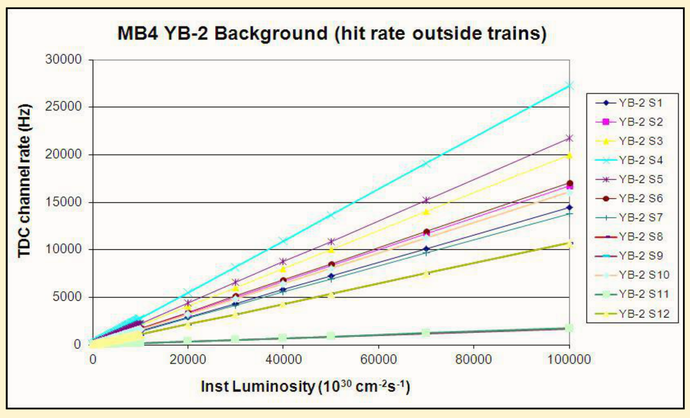
Cristina F. BEDOYA, José Manuel CELA RUIZ*, Álvaro NAVARRO TOBAR, Ignacio REDONDO FERNÁNDEZ
Carlos WILLMOTT ZAPPACOSTA

CIEMAT - Centro de Investigaciones Energéticas, Medioambientales y Tecnológicas
Avda. Complutense, 40 - 28040, Madrid - Spain

ABSTRACT

The first layer of the CMS (Compact Muon Solenoid) DT (Drift Tube) read-out system is built around the ROBs (Read Out Boards), which are responsible for the time measurement of the chamber signals to allow reconstruction of charged particle tracks with a resolution of 250 µm per cell. ROB boards have shown an excellent performance during LHC operation and are expected to continue their operation safely during all LHC running up to 2022.

Present LHC upgrade plans for Phase 2 foresee an increase of instantaneous luminosity up to $5{\cdot}10^{34}$ $cm^{-2} \cdot s^{-1}$ (leveled) which will increase significantly the expected hit rate. Moreover, CMS is studying to increase the Level 1 Accept (L1A) latency of the trigger signal from 3.2 µs to 20 µs to allow including the tracker subdetector information into the Level 1 trigger decision, and also the L1A frequency from 100 kHz maximum to up to 1 MHz, in order to accommodate the increase of trigger rate due to the higher luminosity. ROB operation under such conditions has been studied and tested in the laboratory, and results are presented in this poster.

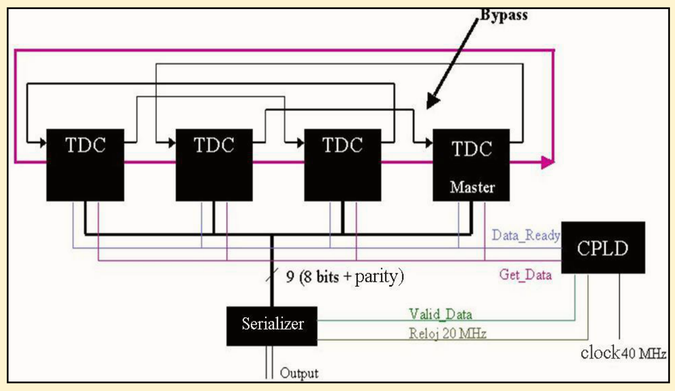


Expected Hit Rate and Read-Out Board Saturation Problem

ROBs are built around a 32-channel HPTDC ASIC developed by the CERN EP/MIC group, with four HPTDCs onto one board, reading up to 128 channels per ROB. Those HPTDCs measure the relative time to a common trigger, for every hit produced on chamber wires, neccesary to reconstruct muon tracks.

The four HPTDCs are connected inside the ROB in a clock synchronous token ring scheme for the read-out of the digital data. One of the HPTDCs is configured as master, controlling the token that authorizes data transmission to a common bus connected to a 240 Mbps serializer –DS92LV1021–.

A failsafe bypassing mechanism has also been implemented in order to guarantee operation of remaining TDCs in case of one failing. An CPLD manages the data_ready/get_data read-out protocol, controlling the handshake between each of the HPTDCs and the serializer. The HPTDC is operated in byte-wise mode at 20 MHz, being the effetive bandwidth of the link 160 Mbps for an estimated throughput of 16 Mbps for LHC nominal operation. This ROB architecture might not be quick enough to cope with the new estimated data and trigger rates.



Experimental Setup

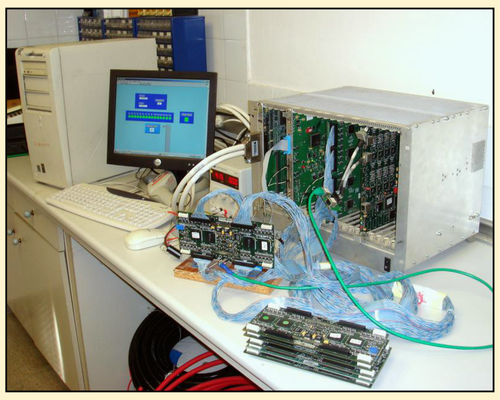
Patgen Board (Fan out 1:128)

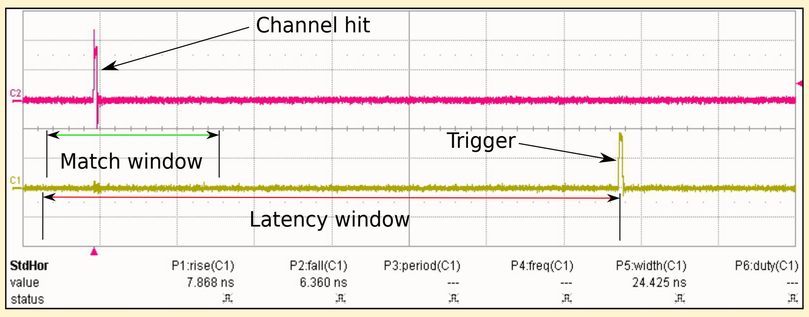
- Two independent input channels; up to 128 outputs that use ROB-inputs compatible standard signalling
- FPGA controller with user-configurable registers: it allows input signal selection, and output channel enabling/disabling.

Control-X Board (Debug and test ROB boards)

Multipurpose VME board. Emulates minicrates control board.

- JTAG lines for configuration and internal monitoring
- Trigger signal generation, simulating CMS L1A signal, with frequency range between 100 kHz and 1.6 MHz
- Capability of delaying an external signal or self-generated trigger signal, to simulate the delay between hits and L1A signal (range: 200 ns - 51.2 µs)
- LHC 40 MHz clock synchronized with the rest of the test stand
- Temperature, current and voltage sensor control lines. Monitoring lines for the power, state or fault of the ROB board





Test Description

The test stand comprises a single ROB board connected to a Control-X and a Patgen boards, and powered by an external power supply.

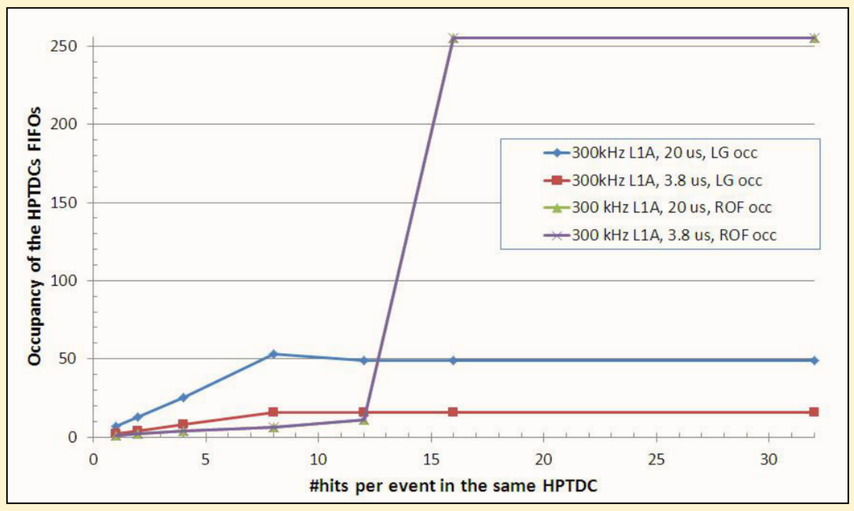
The test procedure consists on emulating DT chambers behaviour, sending hits through different channels, and, after a delay, sending signals representing triggers through the ROB bus. To achieve this, Control-X self-generated periodical signal is forwarded, as a hit pulse, to the Patgen board and, simultaneously, sent to the delay chain, to accomodate within foreseeable future 20 µs latency value. The frequency of both signals is changed step by step, so we can study the impact of different trigger rates in the ROB occupancy. For each test:

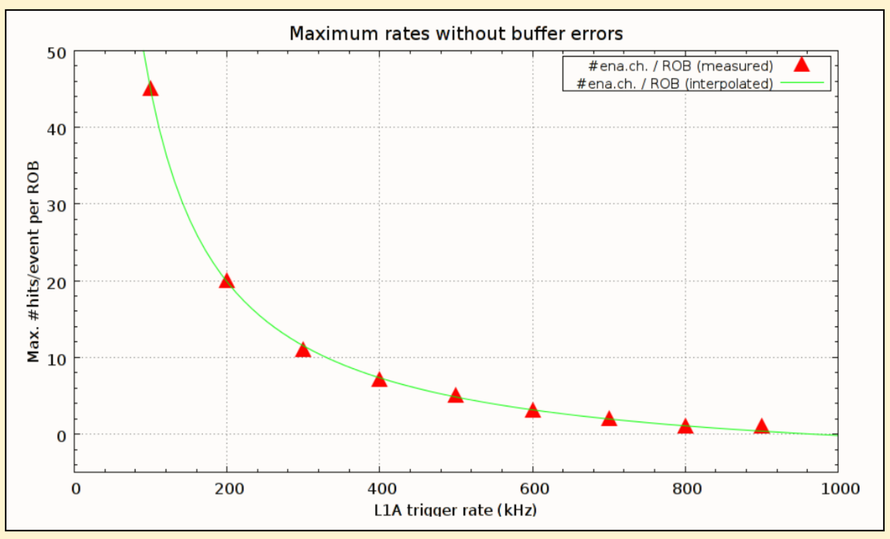
- TDC internal status monitoring and control programs are started
- All hit channels are disabled by Patgen control subprogram
- Control-X powers on the ROB board and sends HPTDC configuration data (20 µs latency)
- ROB board status cheking
- Start sending hit signal at a fixed rate to Patgen. Same signal is delayed and sent as a trigger
- One by one, Patgen channels are enabled until status monitoring program determines a TDC buffer overflow or TDC error
- Test is restarted, changing hit and trigger rate frequency
- Additional tests: enabled channels pattern has been changed, while other parameters remain constant; delay between hits and trigger has also been changed while system running and rest of parameters remain constant
- Total hits per ROB, processed without error or overflow, vs frequency are plotted

Experimental Results

The figure below shows the maximum values achieved, which have been represented as a triangles in the plot. The continuous interpolated curve represents the maximum number of hits that can be processed, per event, versus the L1A trigger rate.

- A dependency between the particular HPTDC where a higher amount of data is read, and the error level generated, has been found, identifying how many TDCs inform about their internal buffer saturation, for each test. Two possible mechanism could be responsible of this bottleneck: inherent differences between different ICs; the round-robin tokenized mechanism used by the TDC chain to decide which device can send its data.
- Repeating all tests with different ROB boards –different groups of TDCs– last effect has also been observed, discarding the differences between ICs as a main bottleneck cause.
- We have verified that the number of hits, at which ROB gives overflow error, is independent from the position of any hit inside the configured time window.
- It has also been checked that the occupancy of the L1A TDC buffer is, in general, low and that the critical point is the read-out FIFO in which already-selected hits are waiting for data transmission over the serial link.





- In theory, up to 500 kHz L1A rate could be achieve for the expected MB4 occupancy at 10^{35} $cm^{-2} \cdot s^{-1}$, but we still need to add the contribution of the track rate –around 10 kHz for the MB4s–. This rate will always include 8 hits per ROB, so in reality, a Level 1 Accept rate higher than 300-400 kHz is not considered safe.

Conclusions

An experimental setup for exploring the throughput limits, that can be achieved by CERN's CMS experiment read-out boards –ROB–, using HPTDCs as digitizer circuits, has been developed. It has shown that there is a monotonically decreasing dependency between the maximum read-out capability of a ROB and the L1A trigger and hit rates. Throughput limits due to round-robin method, used to coordinate different HPTDCs data sending through the board link, have been found one of the major barriers in order to achieve higher read-out data rates. The fact that 4 HPTDCs share the same 240 Mbps serial link, imposes critical constrains to the maximum Level1 Accept rate that can be allowed.

References

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