DEPFET activities at IFIC (Valencia)

IV Jornadas sobre la Participación Española en Futuros Colisionadores

2nd-3rd December, CIEMAT, Madrid

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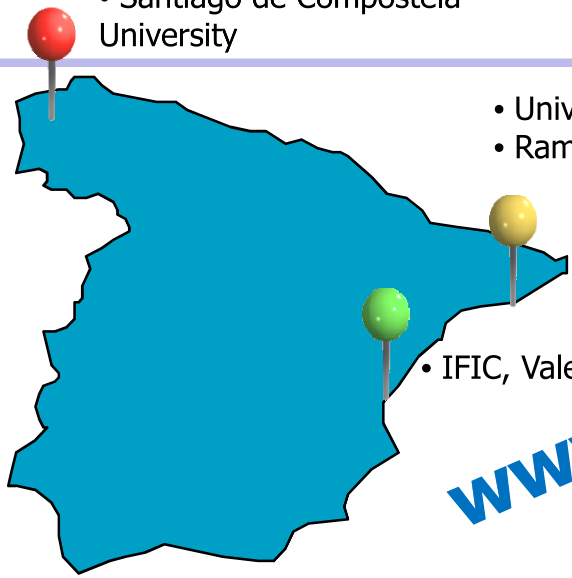
Outlook

- DEPFET: Fundamentals
- New generation of sensors
  - Test Beam 2009
- Thermal and mechanical studies
  - Belle-II
- Conclusions

- Santiago de Compostela University



- University of Barcelona
- Ramon Llull University

- IFIC, Valencia

www.depfet.org

- **University of Barcelona**
- **Ramon Llull University**
- Bonn University
- Heidelberg University
- Goettingen University
- Karlsruhe University
- IFJ PAN, Krakow
- MPI Munich
- Charles University, Prague
- **IGFAE, Santiago de Compostela University**
- **IFIC, CSIC-UVEG, Valencia**
- University of Giessen

Vertexing in future colliders

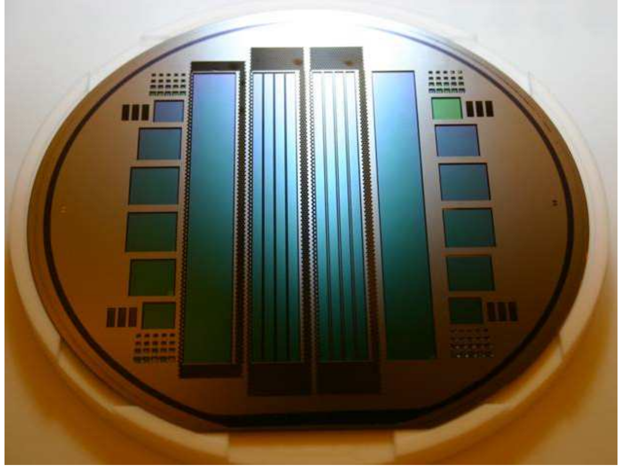
➢ The vertex detectors (VXD) of the future colliders are designed for efficient flavour tagging and vertex reconstruction

➢ This requirements impose unprecedented constraints on the detector:

- Very low material budget
- Fast read-out (low occupancy)
- Good resolution (fine granularity)
- Low power (no active cooling)

DEPFET

➢ Altough this combination of resolution, mass and power is a substantial challenge… Measurements made on realistic DEPFET prototypes have demonstrated that the concept is one of the principal candidates to meet these requirements



From Belle-II to ILC

- Belle-II is an "intermediate point" in our way to the ILC…
  → … but it is more challenging in some points

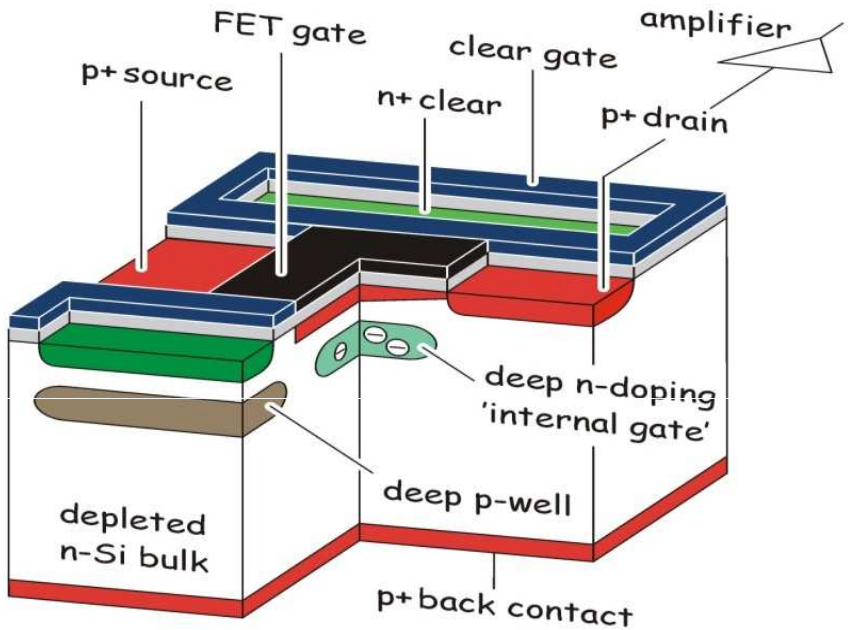
	ILC	Belle-II
Occupancy	0.13 hits/mm^2/s	0.4 hits/mm^2/s
Radiation	< 100 krad/year	> 1Mrad/year
Duty cycle	1/200	1
Frame time	25-100 µs	10 µs
Momentum range	All momenta	Low momentum (< 1 GeV)
Acceptance	6º-174º	17º-150º

- ILC
  - Excellent single point resolution (3-5 µm) → Small pixel size 25µm^2
  - Low material budget (0.12%X_0/layer)

- Belle II
  - Modest spatial resolution (10µm) → Moderate pixel size (50 x 75 µm^2)
  - Few 100 MeV momenta → Lowest possible material budget (0.15% X_0/layer)

DEPFET – DEpleted P-channel Field Effect Transistor

- Each pixel is a p-channel FET integrated on a completely depleted bulk.
- A deep n-implant creates a potential minimum for electrons under the gate (internal gate)



- Signal electrons created in the substrate are accumulated in the internal gate and modulate the transistor current ($g_q \approx 600pA/e^-$)
- Accumulated charge can be removed by a clear contact placed in the periphery of each pixel

- Internal amplification
- Low power consumption: Readout on demand (Sensitive all the time, even in OFF state)

GOAL (ILC)

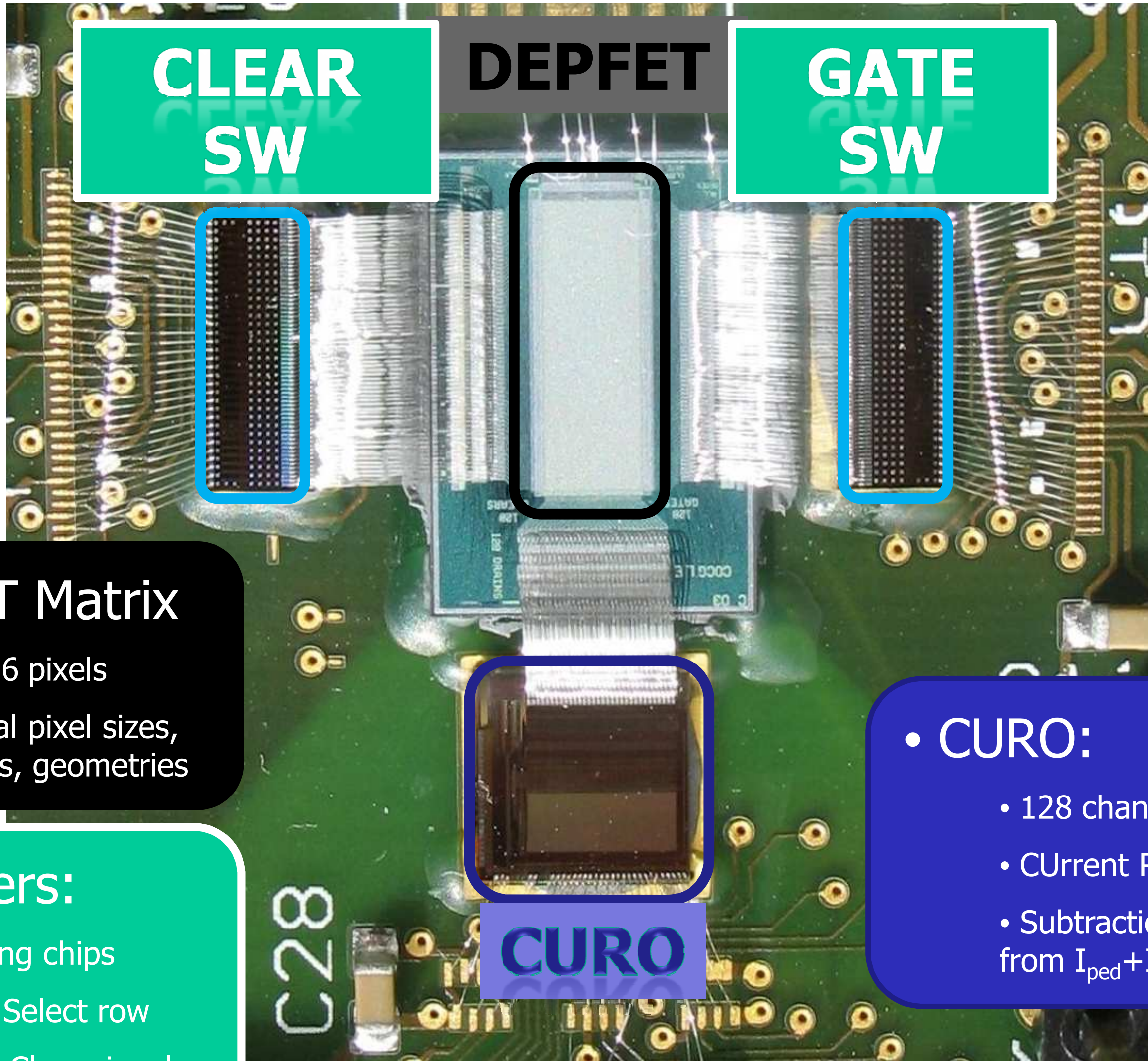
- o Small pixel size ~25µm
- o r/o per row ~50ns (20MHz) (drain)→Fully depleted bulk
- o Noise≈40e^- at high bandwith→Small capacitance and first in-pixel amplification
- o Thin Detectors≈50µm

ILC S3b prototype system

- **Hybrid Board**
  - DEPFET 64x256 matrix
  - Readout chip (CURO)
  - Steering chips (Switchers)

- **S3b Readout Board**
  - ADCs→Digitization
  - FPGA→Chip config. and synchronization during DAQ
  - RAM→Data storage
  - USB 2.0 board→PC comm.

Hybrid board



- DEPFET Matrix
  - 64x256 pixels
  - Several pixel sizes, implants, geometries

- Switchers:
  - Steering chips
  - Gate: Select row
  - Clear: Clear signal

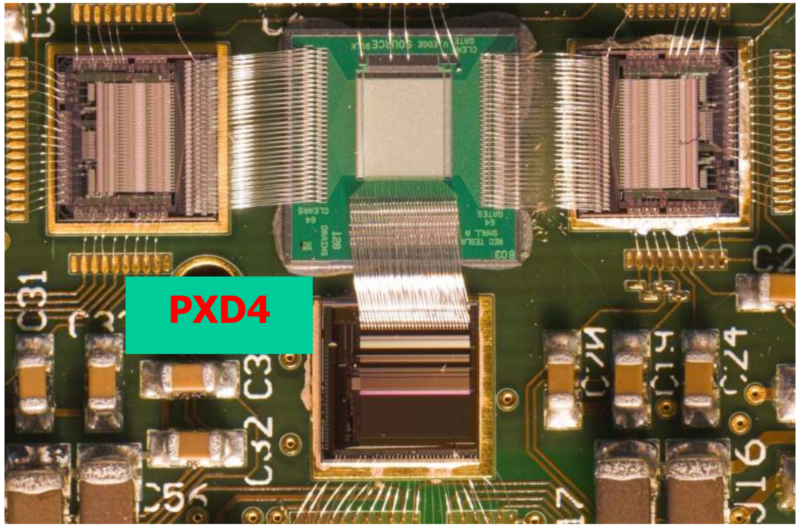
- CURO:
  - 128 channels
  - CUrrent Read Out
  - Subtraction of I_{ped} from $I_{ped}+I_{sig}$

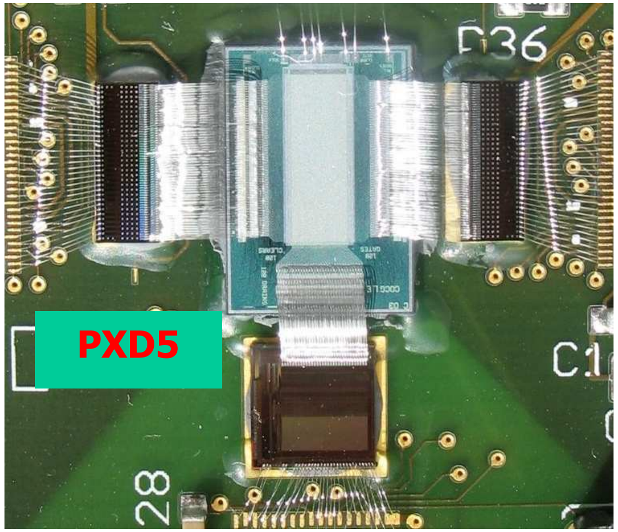
The latest DEPFET Generation 'PXD5'

- ❑ Longer matrices (256x64 pixels)

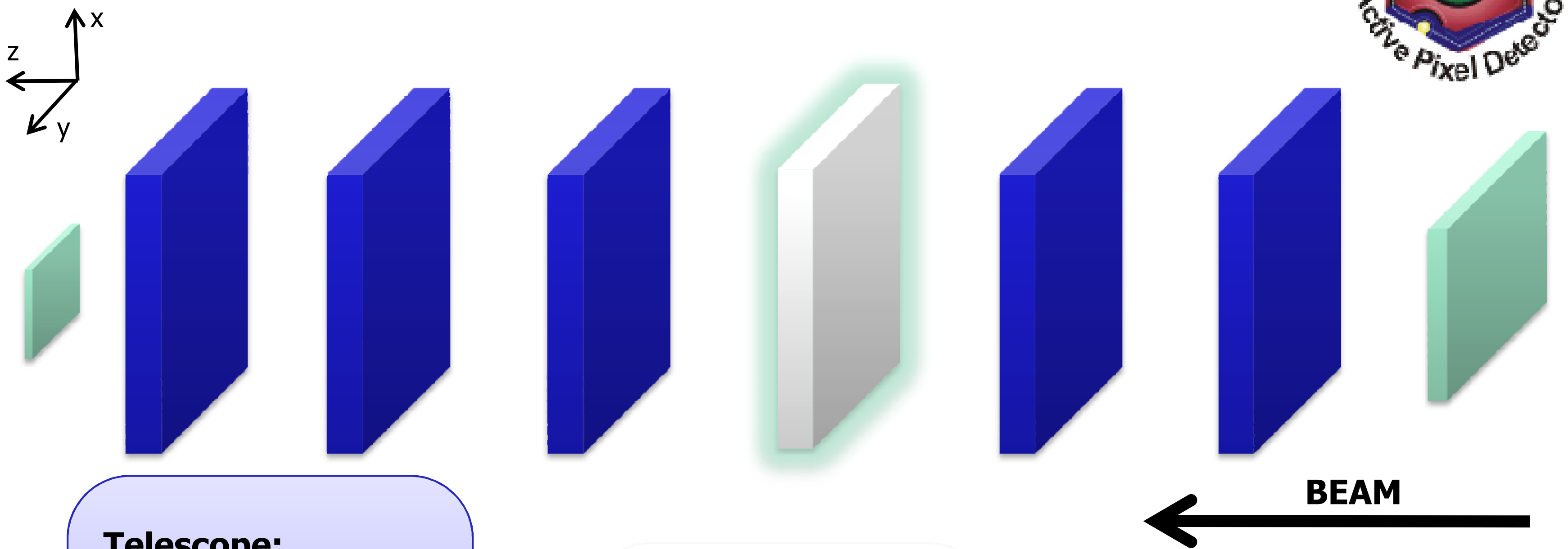
→ **Test Beam 2009 at CERN**
(Coordinator: M. Vos)

- ❑ New DEPFET variants:
  - ✓ Very small pixels (20μm x 20μm)
  - ✓ Capacitively Coupled Clear Gate (C3G) → New step forward in gain
  - ✓ Shorter Gate lengths → Increased internal amplification g_q, (6μm in PXD4; 5 μm in PXD5 → Factor 2 better expected)





Test Beam setup



Telescope:

- 5 DEPFET planes
- 32x24μm^2
- CCG
- 450 μm thick

Trigger Synchronization
via TLU (Trigger Logic Unit)

DUT:

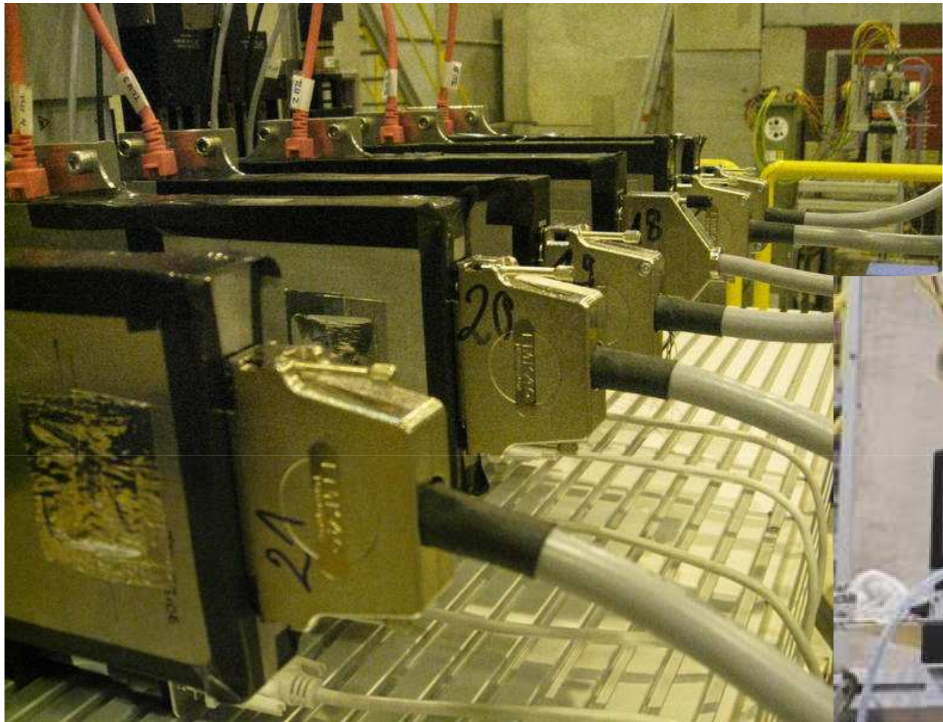
- 1 DEPFET modules
- Various pixel sizes, gate lengths, Clear mechanisms
- 450 μm thick

Scintillators:

- 1 Big "Beam finder"
- 1 Finger "Beam allignment"
- Triggering

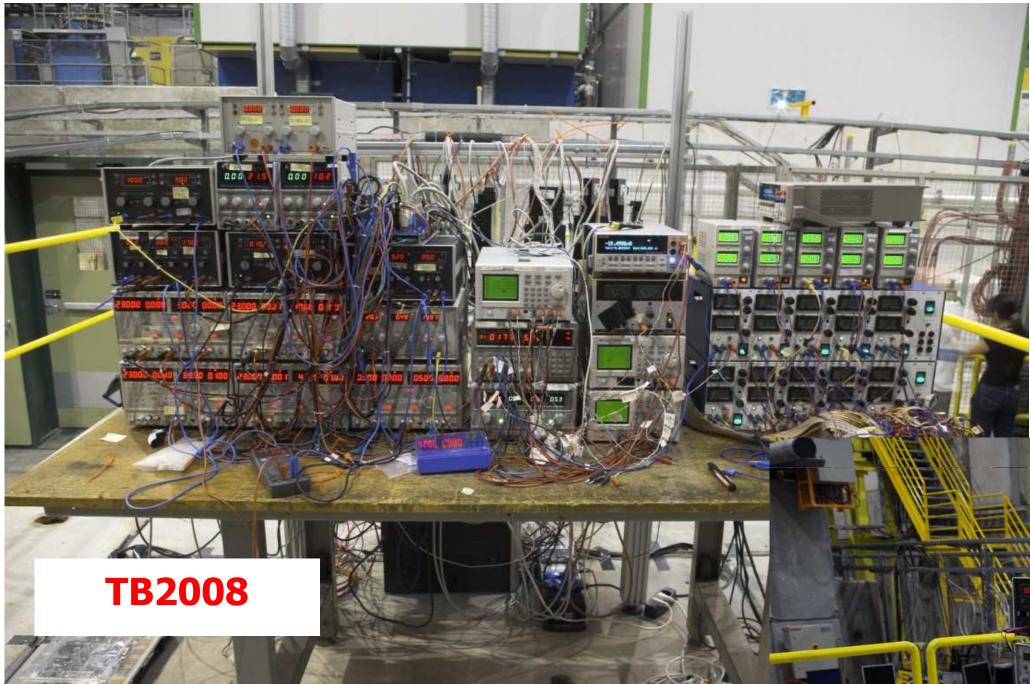
All the modules electrically precharacterized using gamma sources and lasers

Test Beam set-up 2009



✓ Complete measurement programme in the H6 (SPS) line at CERN during 2008 and 2009 campaigns.
✓ EUDET DUT

Test Beam set-up 2009



Simpler design!

- Dedicated DEPFET Power Supplies, one per module
- The complex powering scheme is software controlled

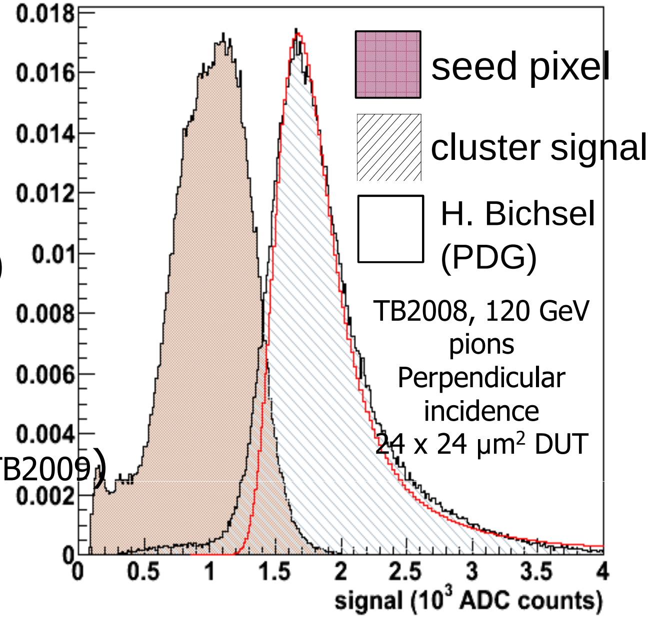
→ Plug-and-play telescope

TB 2008 and 2009 results

- 64x128, 24x24 μm² Common Cleargate (TB2008)
  MPV=1715 ADC counts
  g_q=363pA/e⁻

- 64x256, 32x24 μm² Capacitative Coupled Cleargate (TB2009)
  MPV~2400 ADC counts
  g_q~500pA/e⁻

- 64x256, 20x20 μm² Common Cleargate, $Length_{Gate}$=5μm (TB2009)
  MPV~3100 ADC counts
  g_q~650pA/e⁻ (2x previous g_q, as expected)



Module #	0	1	2	3	4	5
X Residual (μm)	2.9	2.2	2.3	2.0	3.1	3.4
Y Residual (μm)	2.3	1.7	1.7	1.7	2.2	2.6
X Resolution (μm)	2.1	1.6	1.9	1.3	2.6	2.4
Y Resolution (μm)	1.5	1.3	1.2	1.2	1.8	1.7

120 GeV pions, perpendicular incidence, 32x24 μm² telescope + 24x24 μm² DUT (3)

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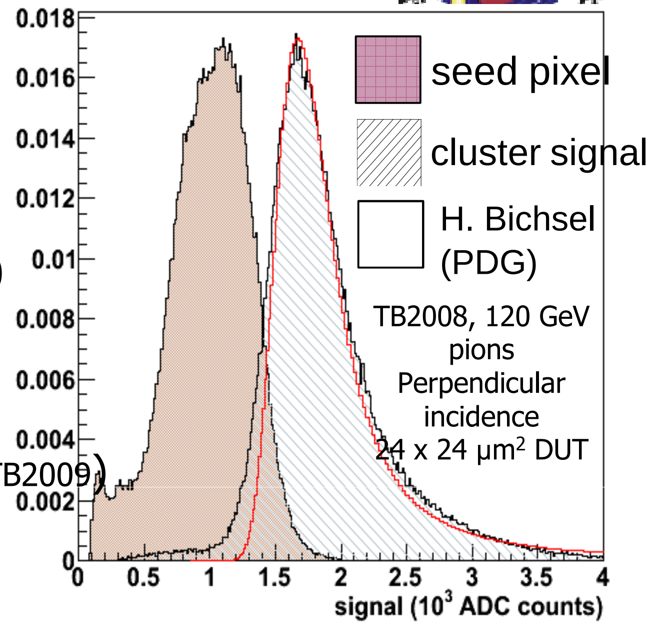

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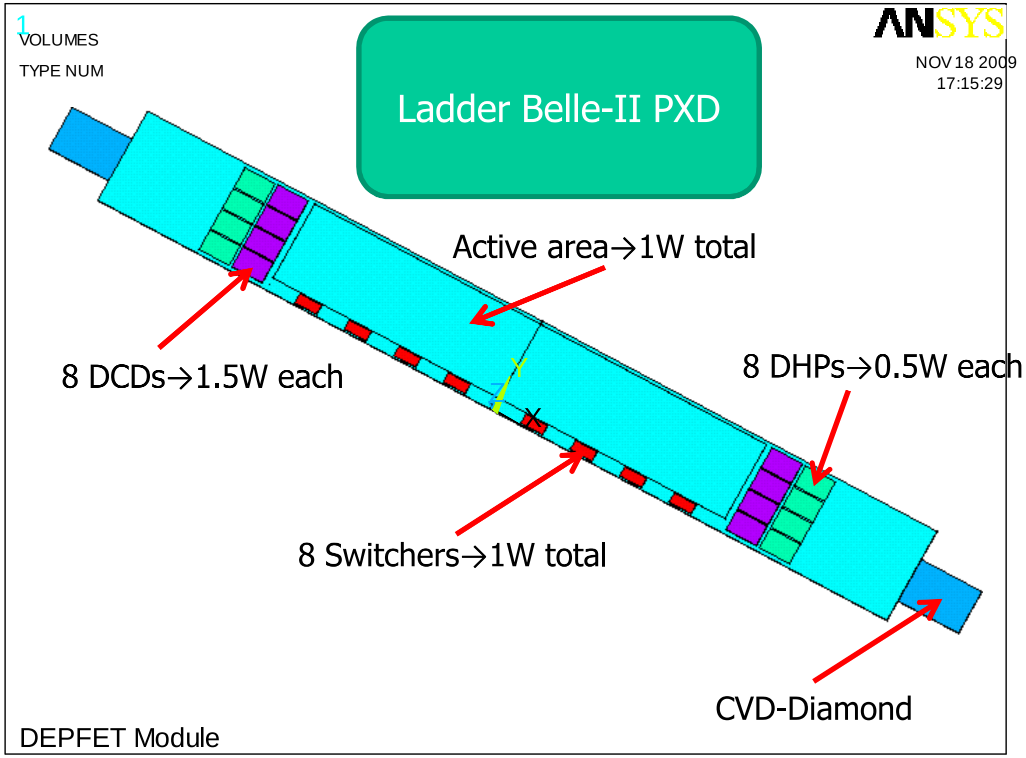
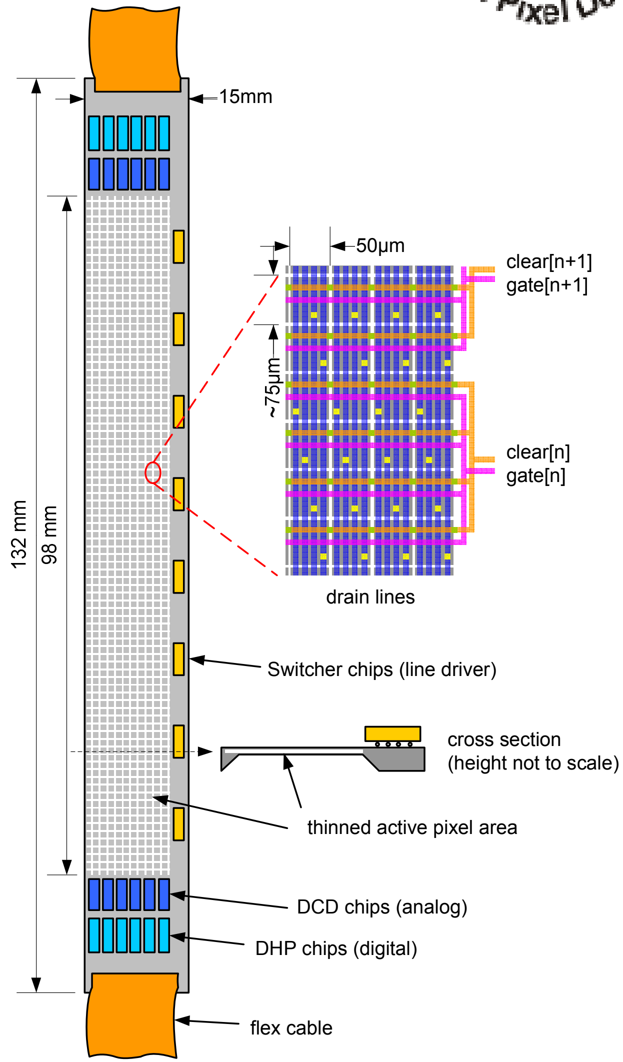
Extremely high resolution

Thermal studies



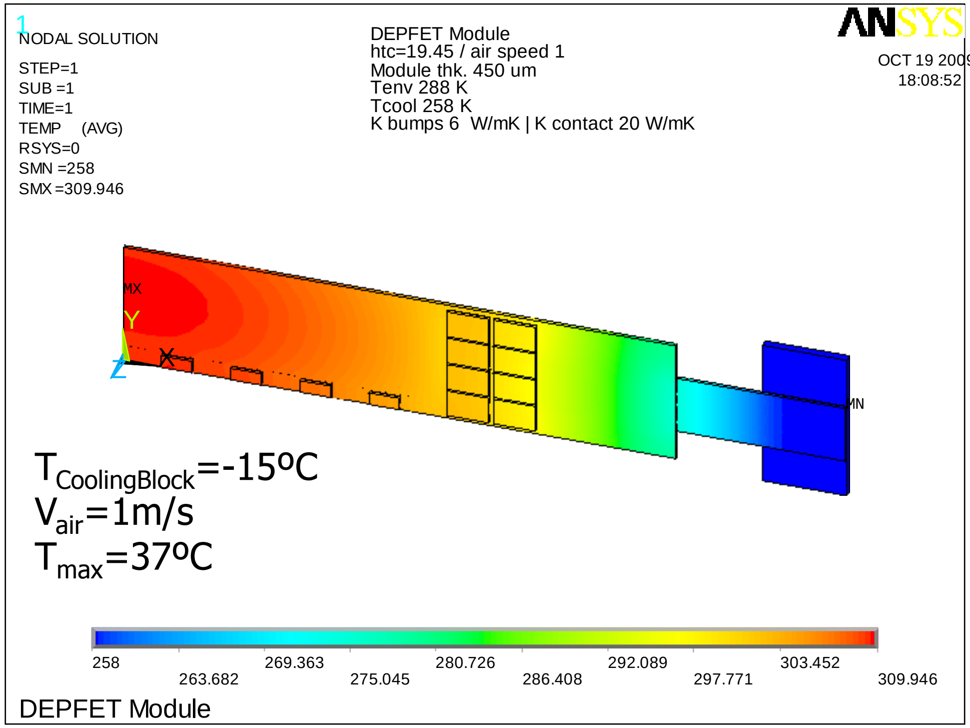


- Full Belle-II ladder implemented in FE software
- Development of cooling options imposing limits on the temperatures:

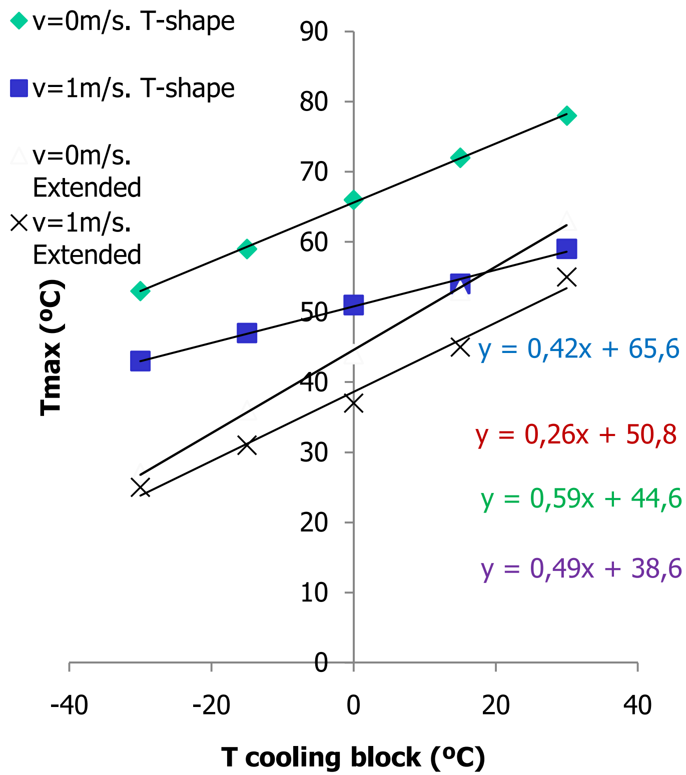
  T_{max} (Sensor)<30ºC

  T_{max} (Chips)<60ºC

Cooling block's temperature



$T_{CoolingBlock}$=-15ºC
V_{air}=1m/s
T_{max}=37ºC

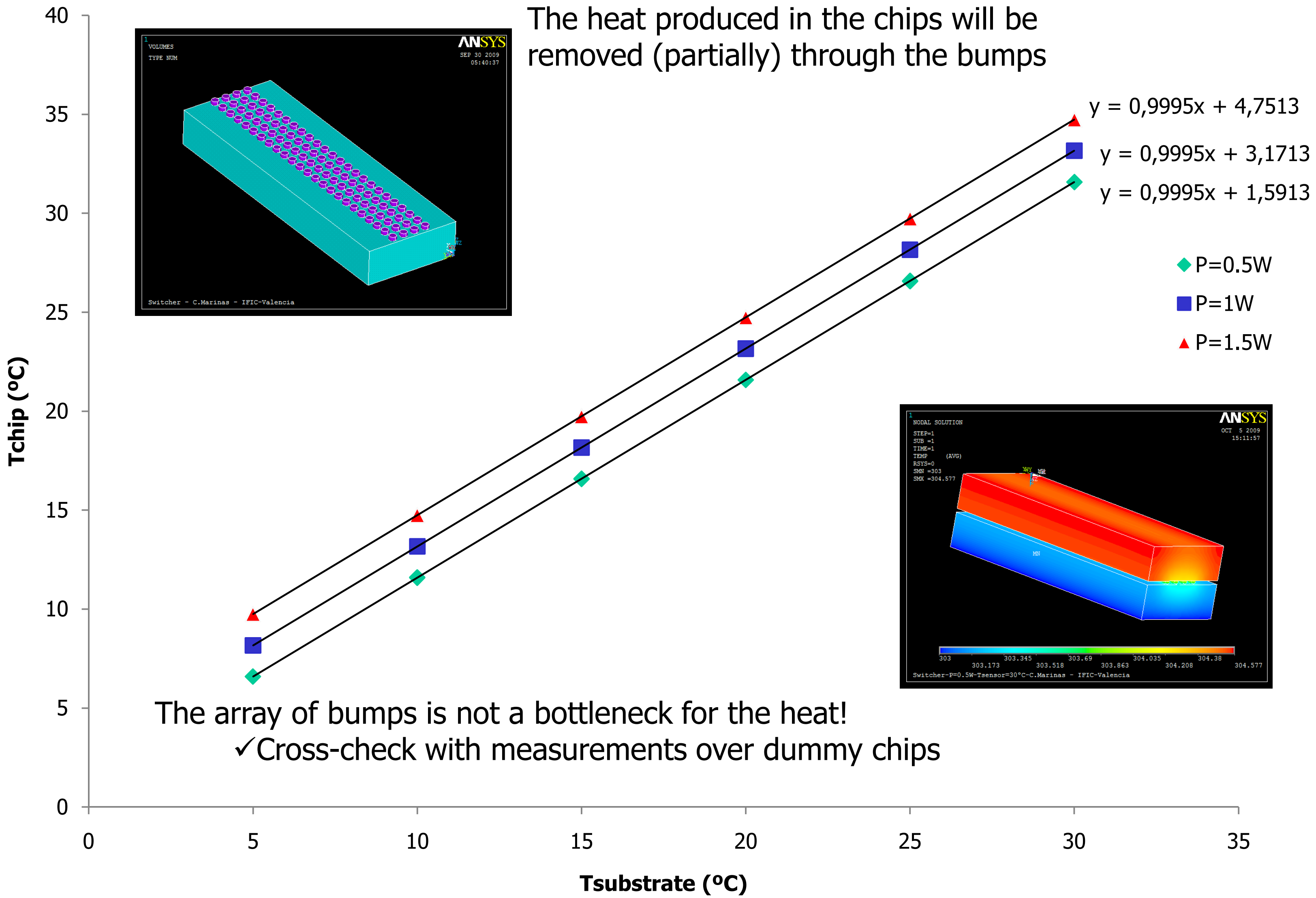


The idea is to fix the many mutually dependant parameters using the simulation (validated with lab. measurements)

- Cooling block's temperature
- Speed and temperature of air
- Diamond bridge length
- …

Solder bumps

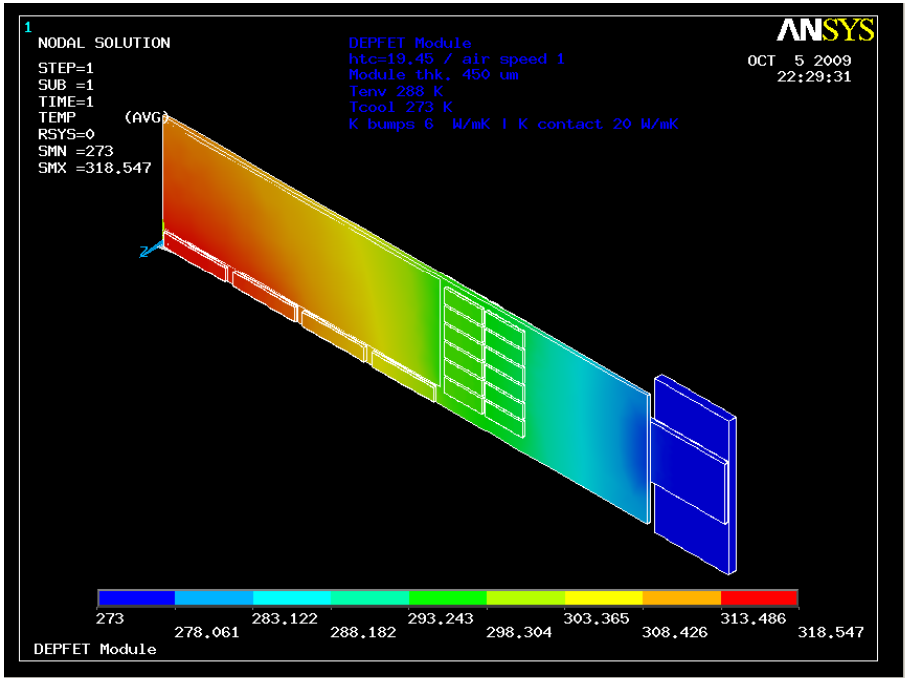
The heat produced in the chips will be removed (partially) through the bumps

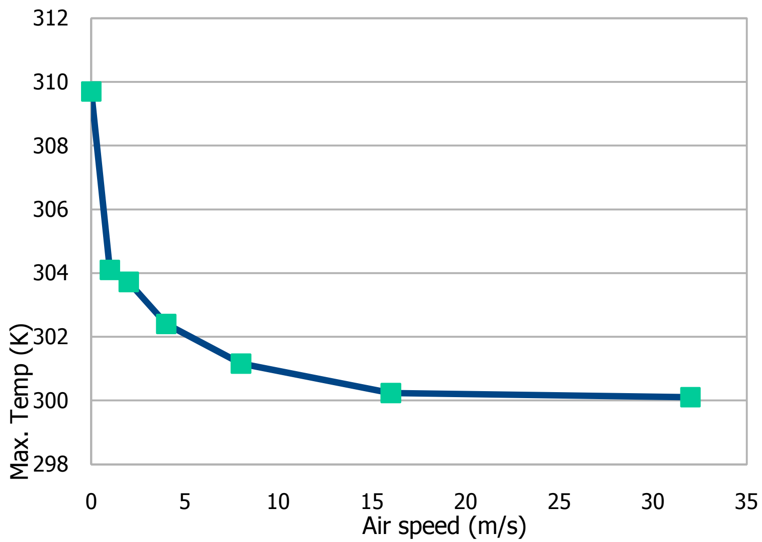


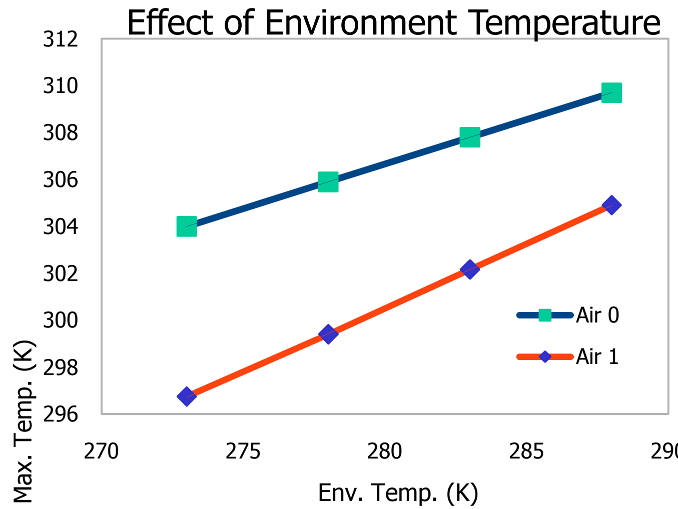
The array of bumps is not a bottleneck for the heat!

✓Cross-check with measurements over dummy chips

Effect of forced convection

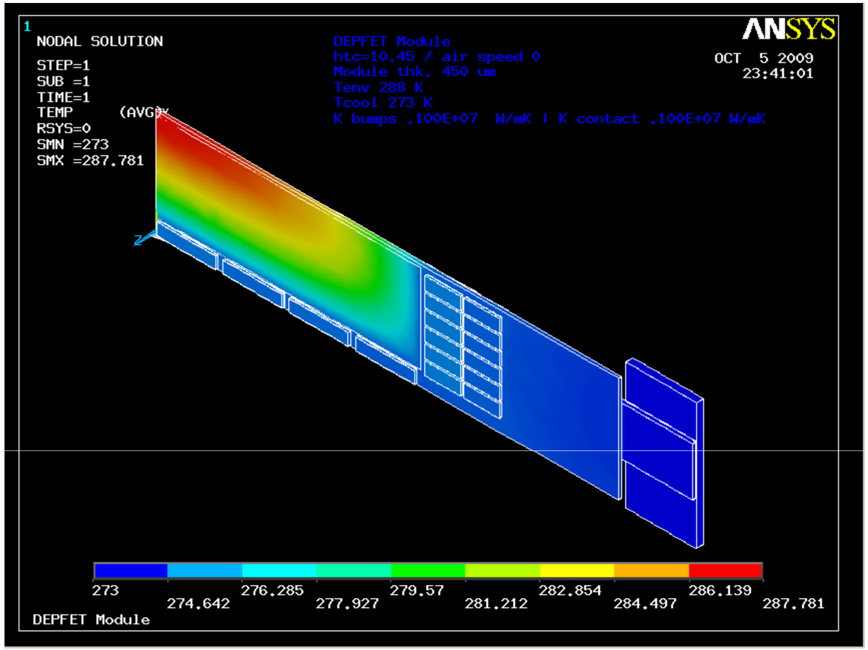


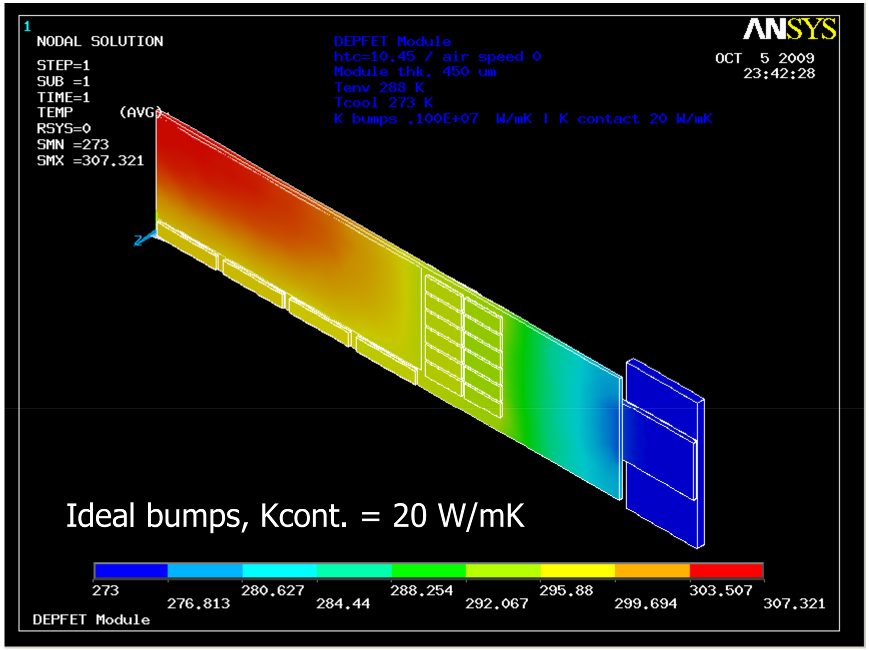


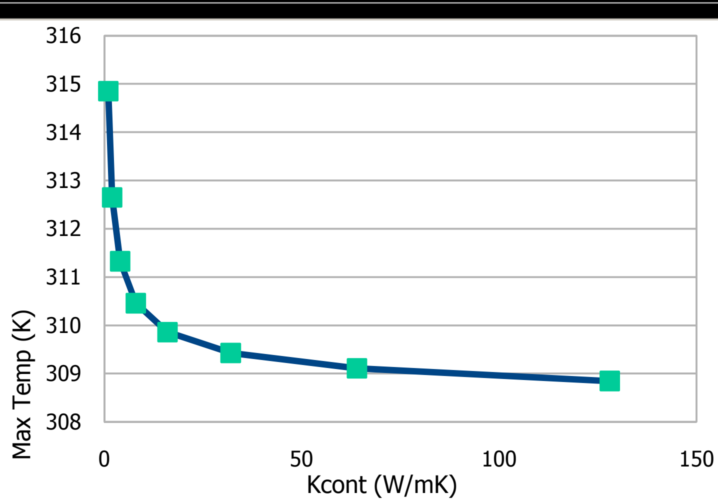


- We just need to "move" the air… no high speed is required!
- Behaviour reproduced in lab. measurements.

Contacts



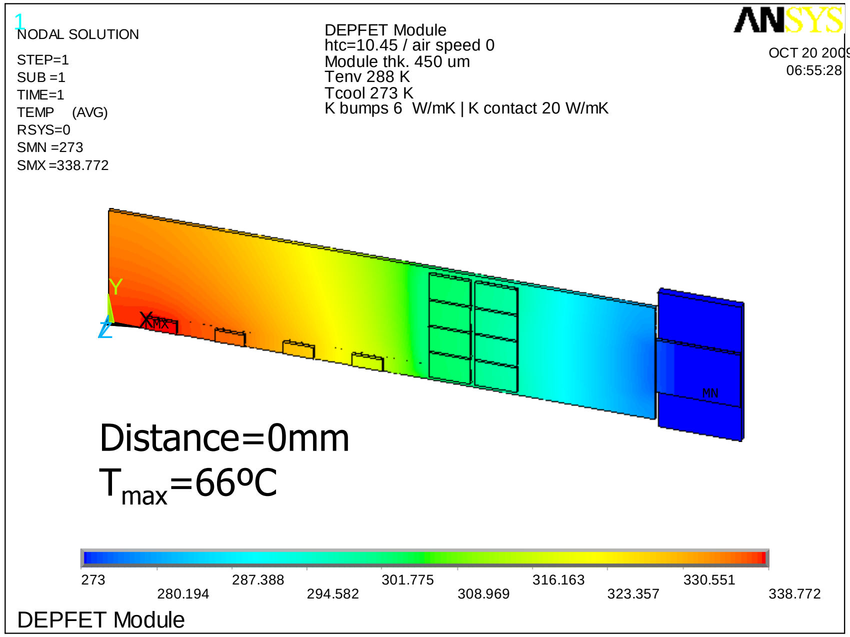


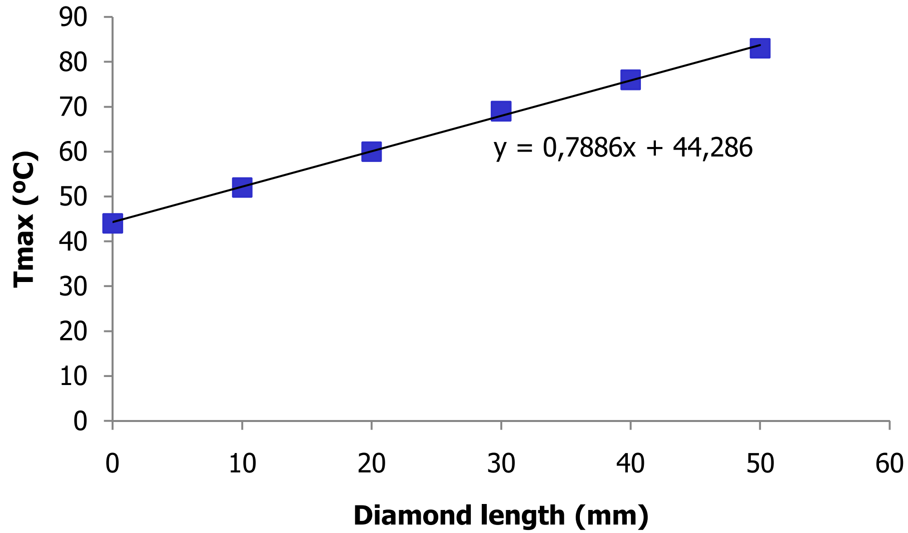


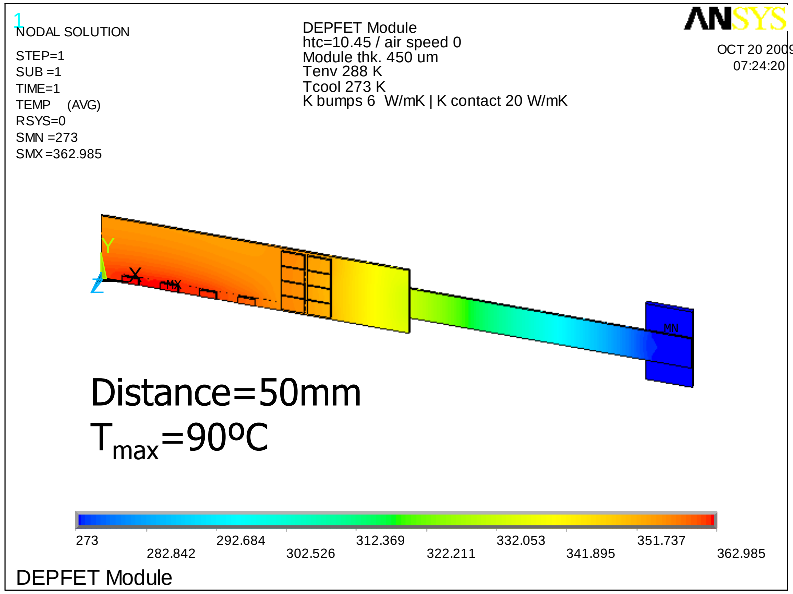
We have discovered that the contacts are not a minor issue…

- Two contacts to be optimized:
  - ➢ Diamond-sensor
  - ➢ Diamond-cooling block

Diamond bridge length



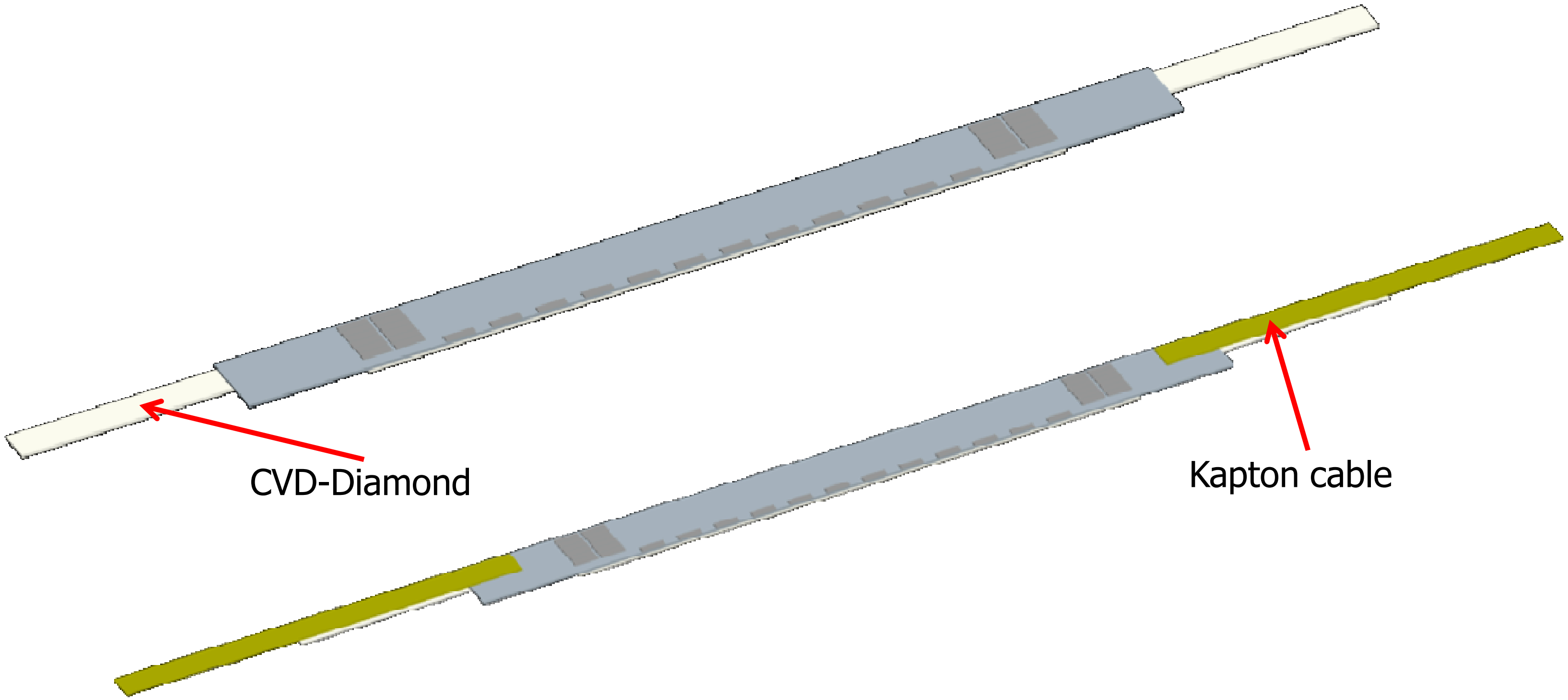




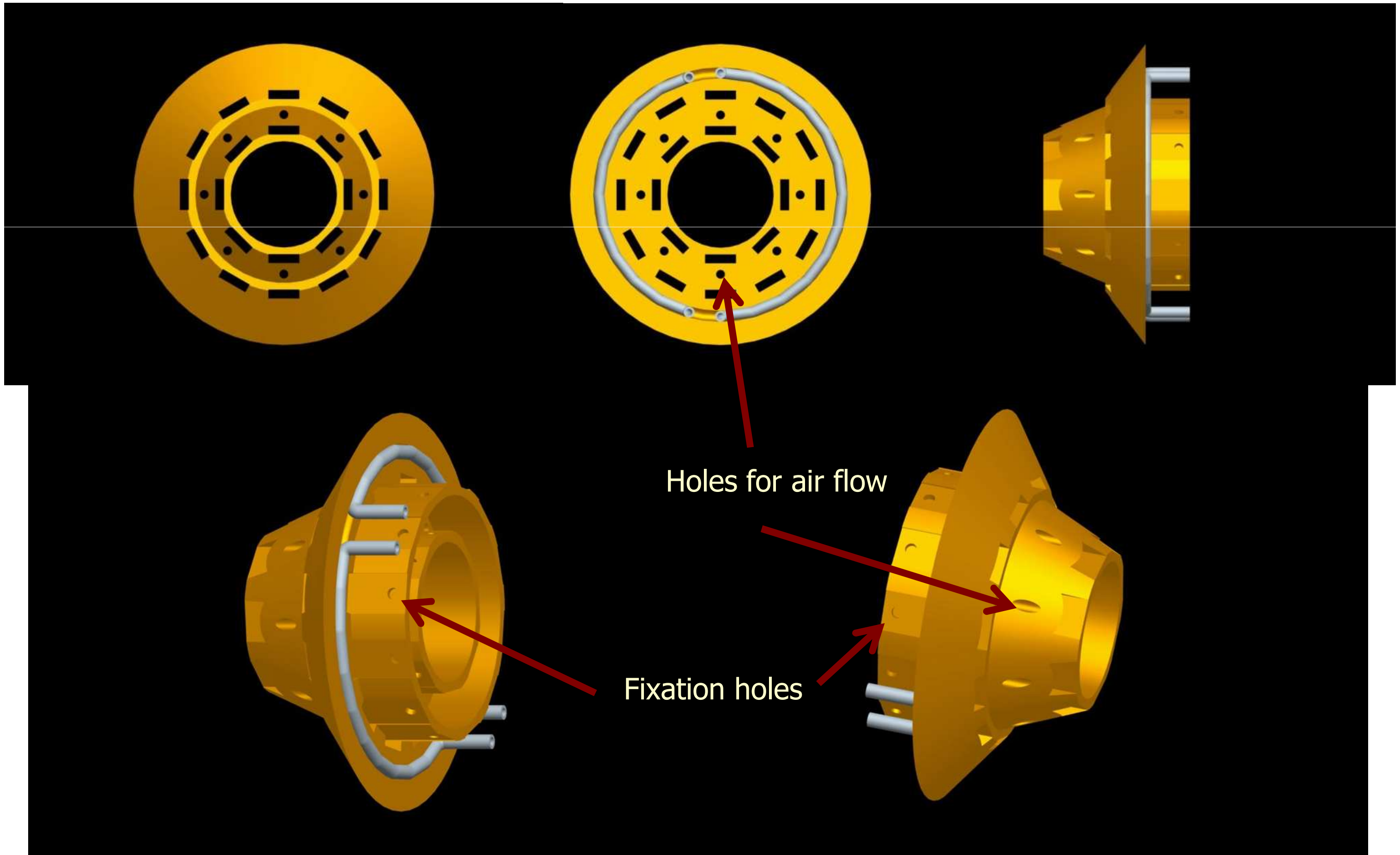
- The shorter, the better (as expected!)
- Key issue on designing the ladder's supports

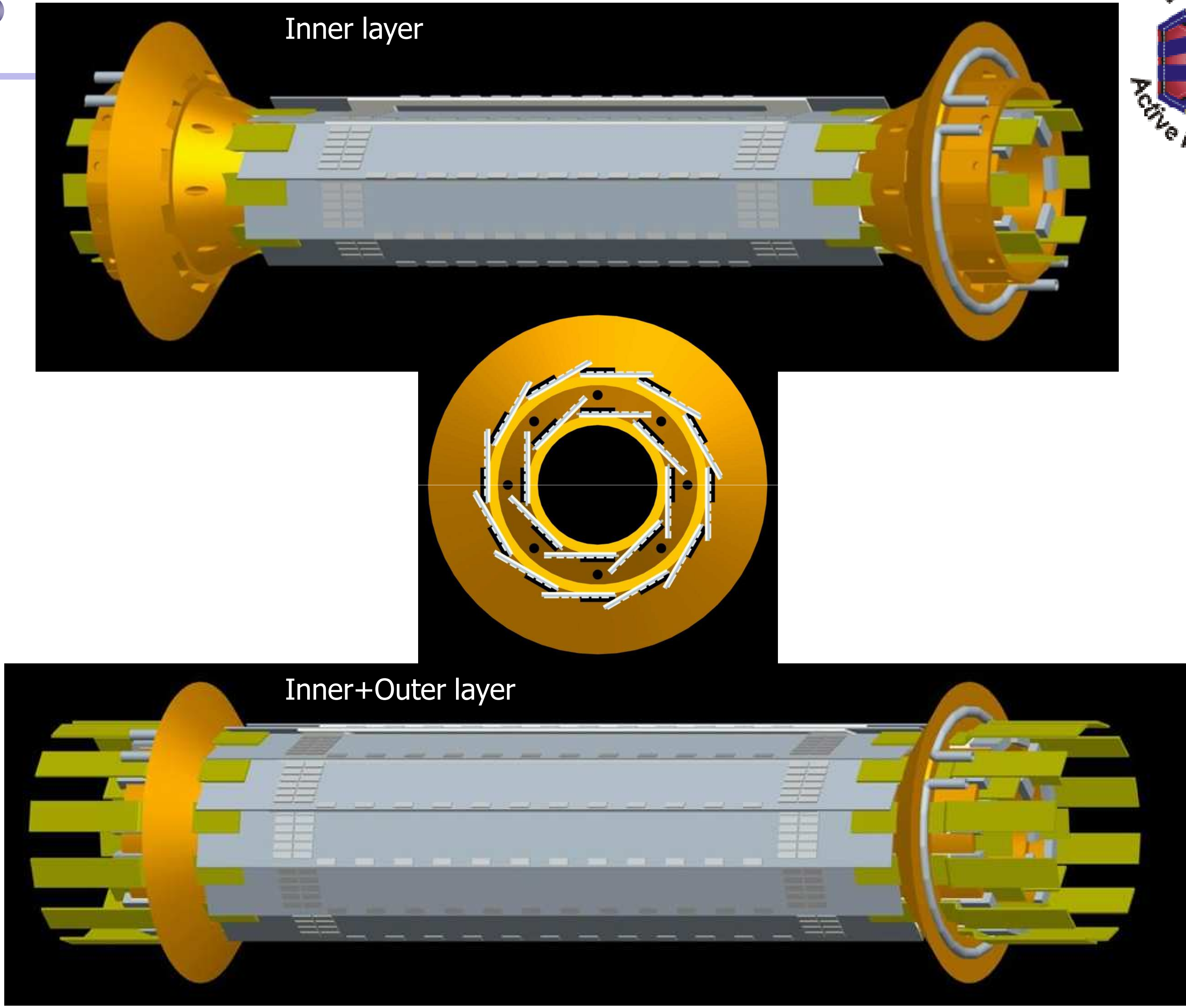
Belle-II PXD Mechanics

Create a structure to support the ladders, cool down the modules and bring air inside the detector



- A "conical" structure split in two shells
  - ➔ Holes (rectangular shape) to pass diamond and cables through
  - ➔ Holes (circular shape) for air flow
  - ➔ Cooling: 2 circuits (one per clam-shell) as a pipe half buried and welded to the structure




Inner layer
Inner+Outer layer

Summary

- General remarks
  - Vertexing in future colliders imposes a combination of good resolution, low material budget and low power consumption → A substantial challenge!
  - DEPFET is one the most promising candidates to meet this requirements
  - Belle-II is not an easy task!
- Test Beam 2009 at CERN
  - New sensors were tested: size x2, higher g_q
  - Improved dedicated power supplies
  - Extremely high resolution (~1um)
- Thermal and mechanical measurements and simulation
  - Development of a simulation tool to fix the cooling parameters
    - Conduction
    - Convection
    - Cooling options
  - Mechanical design of the supports

Belle II TDR (PXD)

- Physics motivation for the PXD and Overview
- Layout of the PXD Detector (General Description)
- DEPFET Sensor, Principles and Production
- Electronics (ASICS)
- Module Assembly and Interconnections
- Figures for the Module Section
- **Mechanical Support and Cooling**
- Power and Services, Interface to Belle-II
- Test Procedures
- Data Acquisition and Data Reduction
- **Test beam results**
- Expected Performance (Optimization Studies)
- Project Organization

To be ready in May 2010

Thank you very much!